

# Tutorial:

## *Model-Based Design Using Model Composer*

UG1259 (v2018.2) June 6, 2018



## Revision History

The following table shows the revision history for this document.

Section	Revision Summary
<b>06/06/2018 Version 2018.2</b>	
General updates	Editorial updates and corrections. Changed all instances of <code>xmcCreateLibrary</code> command to <code>xmcImportFunction</code> command. Command has been renamed to better indicate its function.
<a href="#">Step 2: Custom Blocks with Function Templates</a> (Lab 2)	Added a Step 2 to Lab 2 to create a custom block using function templates.
<b>04/04/2018 Version 2018.1</b>	
General updates	Editorial updates and corrections. Updated dialog box displays throughout manual to reflect appearance in 2018.1 release.
<a href="#">Step 1: Set up the Example</a> (Lab 2)	Added this Note: <b>IMPORTANT:</b> You can use the <code>const</code> qualifier in the function signature to identify the inputs to the block or use the pragma <code>IMPORT</code> .

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## Model Composer Lab Overview

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### Introduction

Xilinx® Model Composer is a model-based design tool that enables rapid design exploration within the Simulink® environment and accelerates the path to production on Xilinx programmable devices through automatic code generation.

Model Composer is designed as an add-on to Simulink and provides a library of performance-optimized blocks for design and implementation of algorithms on Xilinx FPGAs. The Model Composer library offers over 80 predefined blocks, including application-specific blocks for Computer Vision and Image Processing and functional blocks for Math, Linear Algebra, Logic, and Bit-wise operations, among others.

You can focus on expressing algorithms using blocks from the Xilinx Model Composer library as well as custom user-imported blocks, without worrying about implementation specifics, and leverage all the capabilities of Simulink's graphical environment for algorithm design, simulation, and functional verification. Model Composer then transforms your algorithmic specifications to production-quality implementation using automatic optimizations that extend the Xilinx High Level Synthesis technology.

This tutorial introduces the end-to-end workflow for using Model Composer.

The included labs are as follows:

- Lab 1: Introduction to Model Composer
  - Introduction to Model Composer Library Blocks for design
  - Integration with native Simulink and Support for vectors and matrices
  - Working with data types
- Lab 2: Create Custom Blocks in Model Composer
  - Using the `xmcImportFunction` command to specify functions defined in source and header files to import into Model Composer and create Model Composer blocks or a block library.
  - Creating custom blocks with Function templates
- Lab 3: Automatic Code Generation
  - Requirements for Code Generation

- Mapping Interfaces
- Generate an IP for use in the Vivado IP Integrator
- Generate Vivado® HLS Synthesizable Code
- Port a Model Composer Synthesized Design into System Generator for DSP

## Software Requirements

The lab exercises in this tutorial require that you have installed the following software:

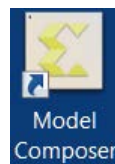
- MATLAB™: The MATLAB releases and simulation tools supported in this release of Model Composer are described in the Compatible Third-Party Tools section of the *Vivado Design Suite User Guide: Release Notes, Installation, and Licensing* (UG973).
- Vivado Design Suite release: 2018.2 (Includes Vivado HLS)
- Model Composer: 2018.2

See the *Vivado Design Suite User Guide: Release Notes, Installation, and Licensing* (UG973) for a complete list and description of the system and software requirements

## Launching Model Composer

To launch Model Composer:

- On Windows systems:
    - Select **Start > All Programs > Xilinx Design Tools > Model Composer 2018.x > Model Composer 2018.x**.
- OR
- Double-click the Model Composer icon which was placed on your desktop after installation.



- On Linux systems:
 

You launch Model Composer under Linux using a shell script called `model_composer` located in the `<Model_composer_install_dir>/2018.x/bin` directory. Before launching this script, you must make sure the MATLAB executable can be found in your Linux system's `$PATH` environment variable for your Linux system. When you execute the `model_composer` script, it will launch the first MATLAB executable found in `$PATH` and attach Model Composer to that session of MATLAB. Also, the `model_composer` shell script supports all the options that

MATLAB supports and all options can be passed as command line arguments to the `model_composer` script.

When Model Composer opens, you can confirm the version of MATLAB to which Model Composer is attached by entering the `version` command in the MATLAB Command Window.

```
>> version
ans =
    '9.2.0.538062 (R2017a)'
```

## Locating and Preparing the Tutorial Files

There are separate project files and sources for each of the labs in this tutorial. You can find the design files for this tutorial on the [www.xilinx.com](http://www.xilinx.com) website.

1. **Download** the [Reference Design Files](#) from the Xilinx website.
2. **Extract** the zip file contents into any write-accessible location on your hard drive or network location.



**RECOMMENDED:** You will modify the tutorial design data while working through this tutorial. You should use a new copy of the `ModelComposer_Tutorial` directory extracted from `ug1259-model-composer-tutorial.zip` each time you start this tutorial.



**TIP:** This document assumes the tutorial files are stored at `C:\ModelComposer_Tutorial`. All pathnames and figures in this document refer to this pathname. If you choose to store the tutorial in another location, adjust the pathnames accordingly.



**TIP:** Make sure to save the tutorial files in a folder structure with no spaces in them. There is a known limitation that does not support spaces in the directory structure for code generation.

### Introduction

This tutorial shows how you can use Model Composer for rapid algorithm design and simulation in the Simulink<sup>®</sup> environment.

### ***Procedure***

This lab has the following steps:


- In Step 1, you examine the Model Composer Simulink library.
- In Step 2, you build a simple design using Model Composer blocks to see how Model Composer blocks integrate with native Simulink blocks and supported Signal Dimensions.
- In Step 3, you look at data types supported by Model Composer and the conversion between data types.

## Step 1: Review the Model Composer Library

In this step you see how Model Composer fits into the Simulink environment, and then review the categories of blocks available in the Model Composer library.

### Access Model Composer Library

Model Composer provides 80+ blocks for use within the Simulink environment that you can access them from within the Simulink Library Browser:

1. Use any of these techniques to open the Simulink Library Browser:
  - a. On the Home tab, click **Simulink**, and choose a model template. In the new model, click the **Library Browser** button. 
  - b. At the command prompt, type:
 

```
slLibraryBrowser
```
2. In the browser, navigate to the **Xilinx Model Composer** library.

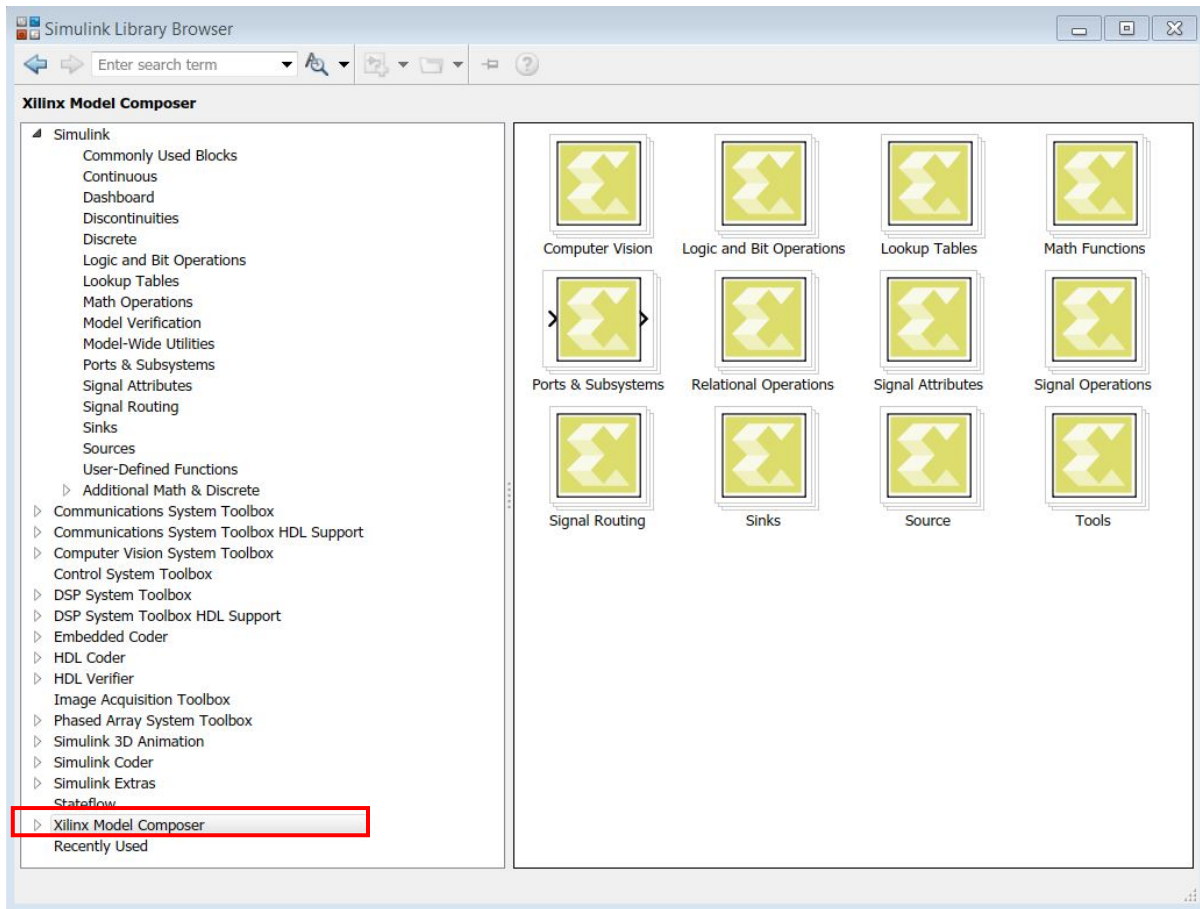


Figure 1: Xilinx Model Composer Library

The Model Composer blocks are organized into subcategories based on functionality. Spend a few minutes navigating through the sub-libraries and familiarizing yourself with the available blocks.

## Step 2: Build Designs with Model Composer Blocks

In this step, you build a simple design using the existing Model Composer blocks.

### *Sobel Edge Detection: Algorithm Overview*

Sobel edge detection is a classical algorithm in the field of image and video processing for the extraction of object edges. Edge detection using Sobel operators works on the premise of computing an estimate of the first derivative of an image to extract edge information.

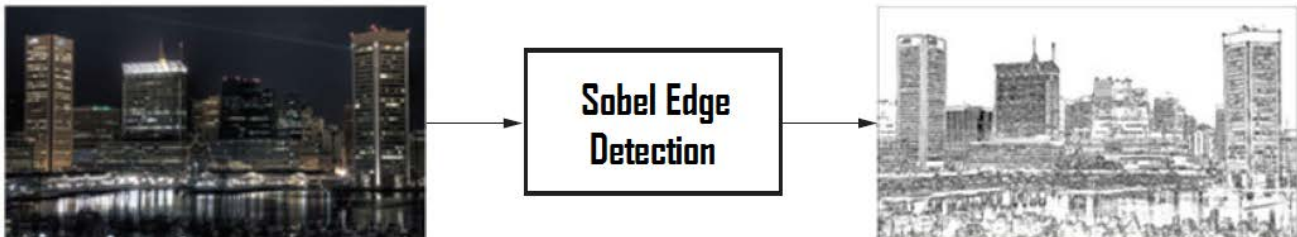


Figure 2: Sobel Edge Detection

### *Implementing Algorithm in Model Composer*

1. In the MATLAB `Current Folder`, navigate to `ModelComposer_Tutorial\Lab1\Section1`.
2. Double-click the `Sobel_EdgeDetection_start.slx` model.

This model already contains source and sink blocks (from Simulink's **Computer Vision System Toolbox**), to stream video files as input directly into your algorithm and view the results. The model also contains some of the needed Model Composer blocks required for this section. Note the difference in appearance for the Model Composer blocks in the design versus the Simulink blocks.

3. From the Library Browser, select the **Sobel Filter** block from the **Computer Vision** sub-library of the Xilinx Model Composer library. Drag the block into the area labeled **Convolve Image Frame with Sobel Kernel and Compute Gradient** as shown in Figure 4 and connect the input of this block to the output of the **From Multimedia File** block.

**Note:** You can also add Model Composer blocks directly into your model by typing the block name onto the canvas (same as Simulink blocks).

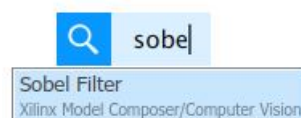
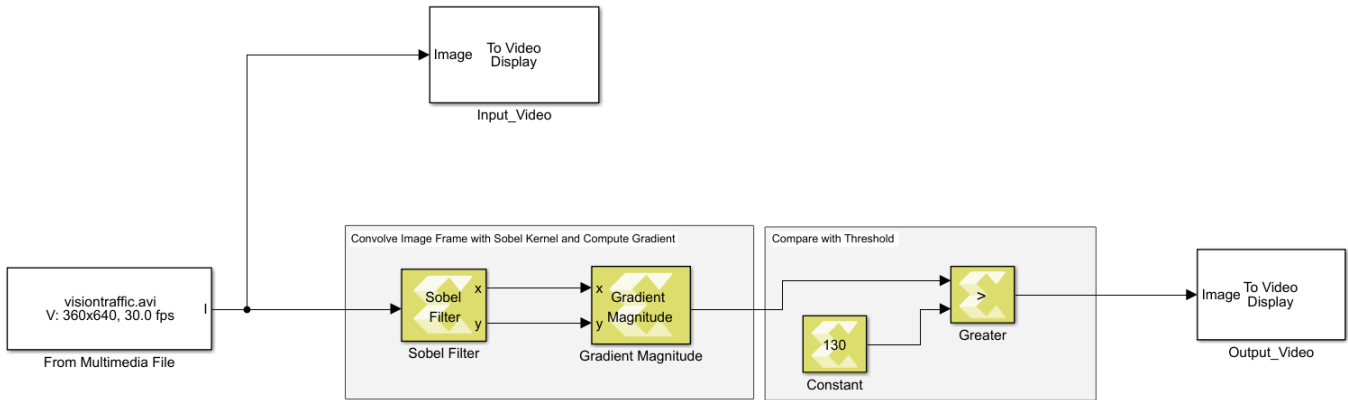


Figure 3: Searching for Sobel Filter Block

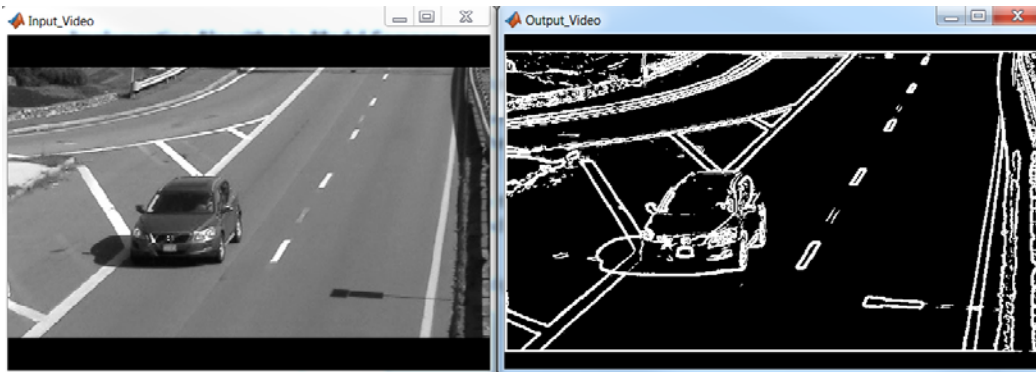
4. From the Library Browser, select the **Gradient Magnitude** block from the Xilinx Model Composer library (also found in the **Computer Vision** sub-library), drag it into the model, and connect the X and Y outputs of the **Sobel Filter** block to the input of this block.
5. Connect the rest of the blocks to complete the algorithm as shown in the following figure:



**Figure 4: Algorithm with Sobel Filter and Gradient Magnitude**

6. Select the **Simulation > Run** command or click the  button to simulate the model and view the results of the Sobel Edge Detection algorithm.

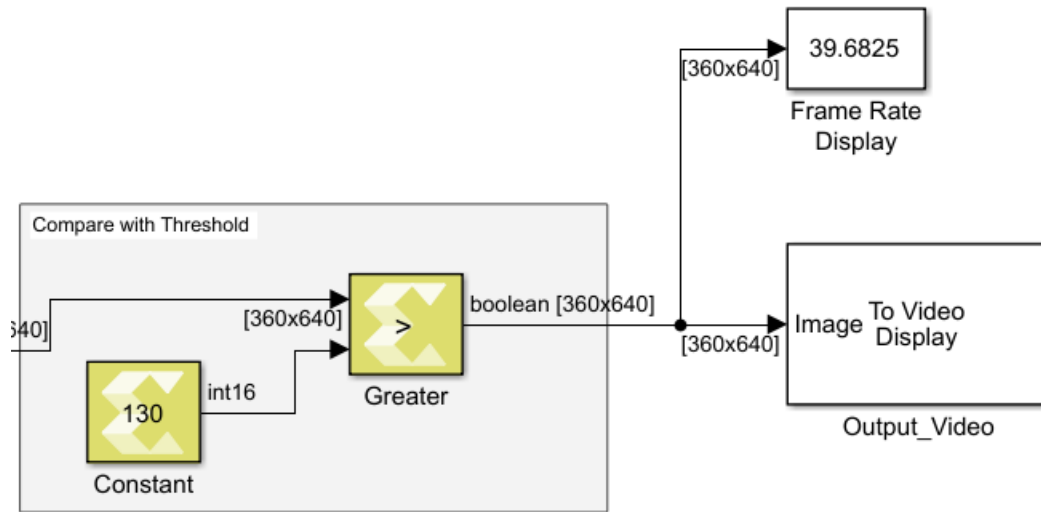
*Note: The Model Composer blocks can operate on matrices (image frames in the following figure).*



**Figure 5: Input and Output Videos**

One way to assess the simulation performance of the algorithm is to check the video frame rate of the simulation. To do this:

7. Add the **Frame Rate Display** block from the Simulink **Computer Vision System Toolbox** (under the **Sinks** category) and connect it to the output of the algorithm as shown in [Figure 6](#).
8. Simulate the model again to see the number of video frames processed per second.



**Figure 6: Frames Processed Per Second**

9. Try these things:

- Change the input video through the **From Multimedia File** block by double-clicking the block and changing the **File Name** field to select a different video. Notice that changing the video resolution in the Source block does not require any structural modifications to the algorithm itself.

**Note:** You must stop simulation before you can change the input file. Also, the .mp4 files in the Matlab vision data tool box directory are not supported.

- Build any variations using other available blocks in the **Computer Vision** sub-library in Model Composer.

**Note:** You can find other smaller examples for reference in the folder `ModelComposer_Tutorial\Lab1\Section1\Examples`

## Step 3: Work with Data Types

In this step, you become familiar with the supported Data Types for Model Composer and conversion from floating to fixed-point types.

This exercise has two primary parts, and one optional part:

- Review a simple floating-point algorithm using Model Composer.
- Look at Data Type Conversions in Model Composer designs.

## Work with Native Simulink Data Types

1. In the MATLAB Current Folder, navigate to the ModelComposer\_Tutorial\Lab1\Section2 folder.
2. Double-click ColorSpace\_Conversion.slx to open the design.  
This is a Color Space conversion design, built with basic Model Composer blocks, that performs a RGB to YCbCr conversion.
3. Update the model (**Ctrl+D**) and observe that the Data Types, Signal Dimensions and Sample Times from the Source blocks in Simulink all propagate through the Model Composer blocks. Note that the design uses single precision floating point data types.
4. Simulate the model and observe the results from simulation.

## Convert Data Types

To convert the previous design to use Xilinx Fixed Point types:

**Note:** Fixed point representation helps to achieve optimal resource usage and performance for a usually acceptable trade-off in precision, depending on the dataset/algorithm.

1. Double-click ColorSpace\_Conversion\_fixed\_start.slx in the Current Folder to open the design.
2. Open the **Xilinx Model Composer** library in the Simulink Library Browser.
3. Navigate to the Signal Attributes sub-library, select the **Data Type Conversion** block, and drag it into the empty slots in the designs, before and after the **RGB to YCbCr** subsystem.

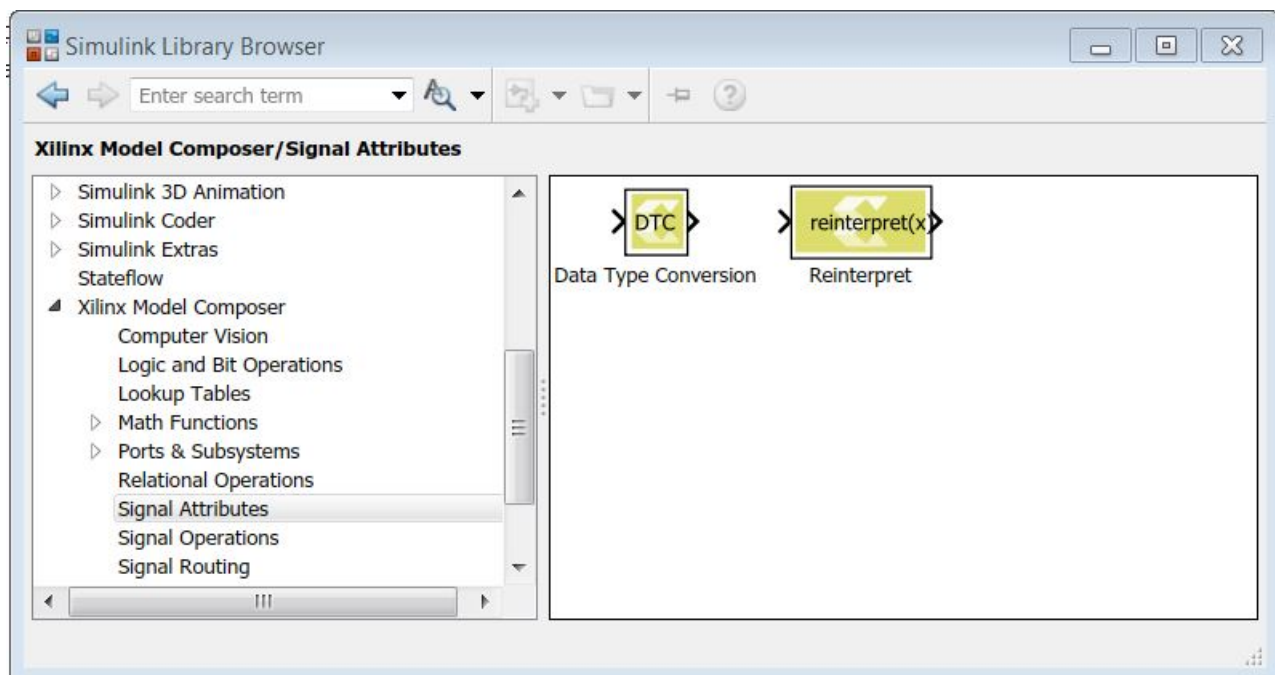
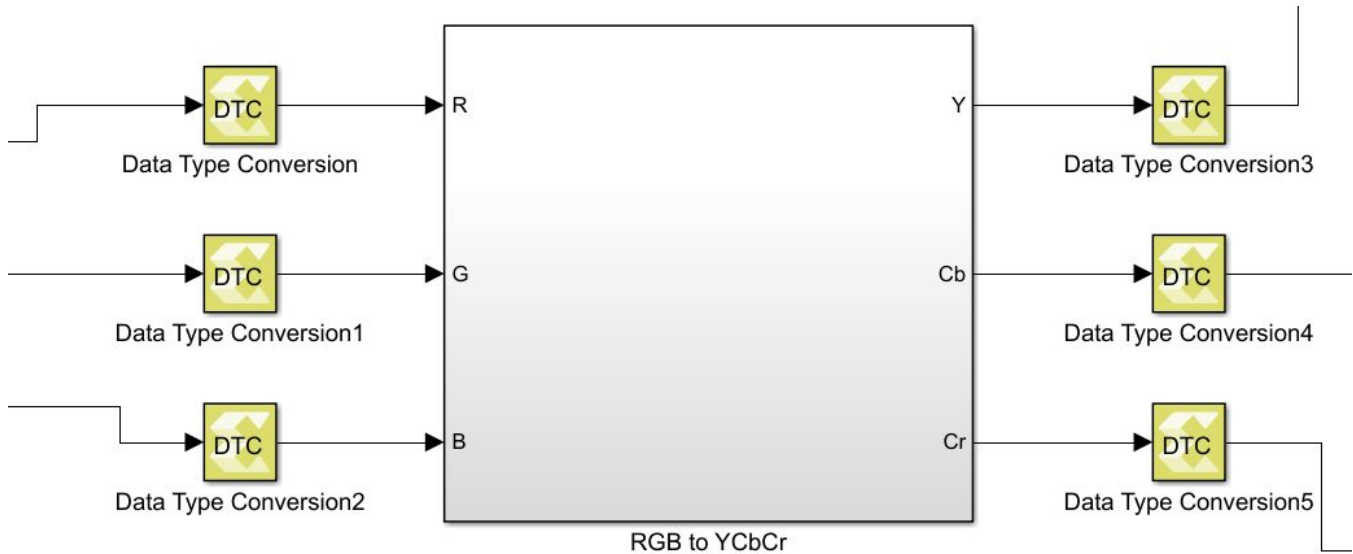
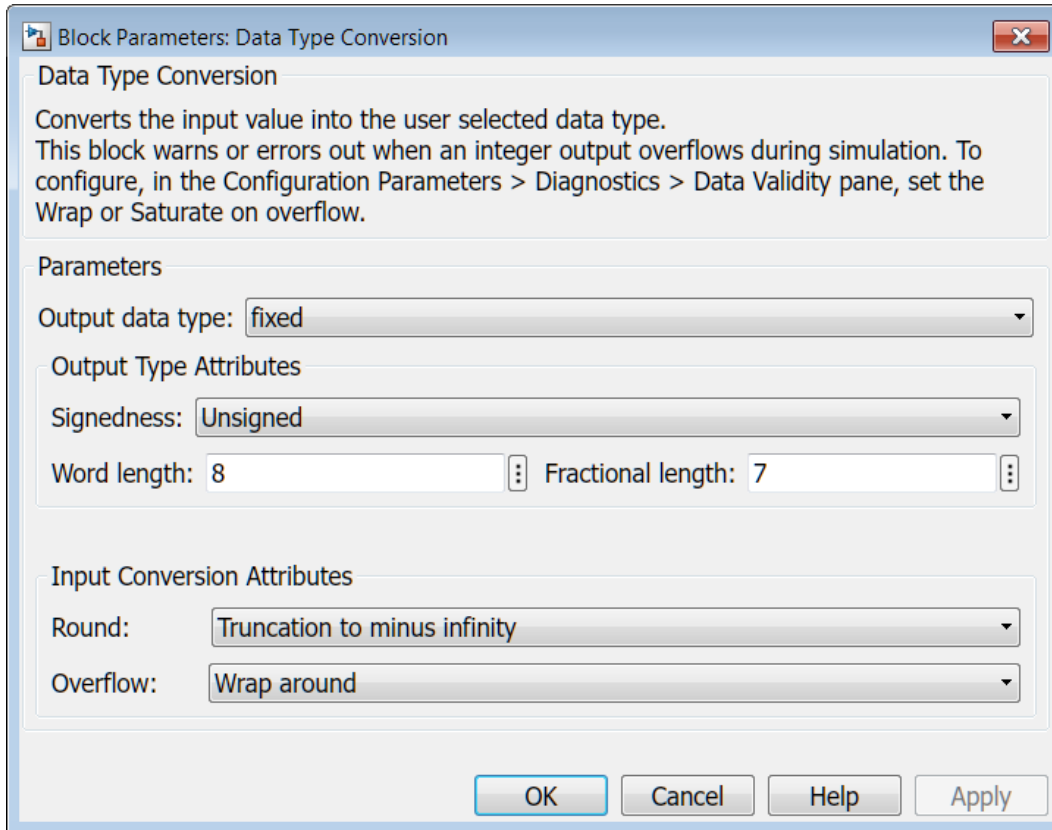


Figure 7: Model Composer Data Type Conversion Block



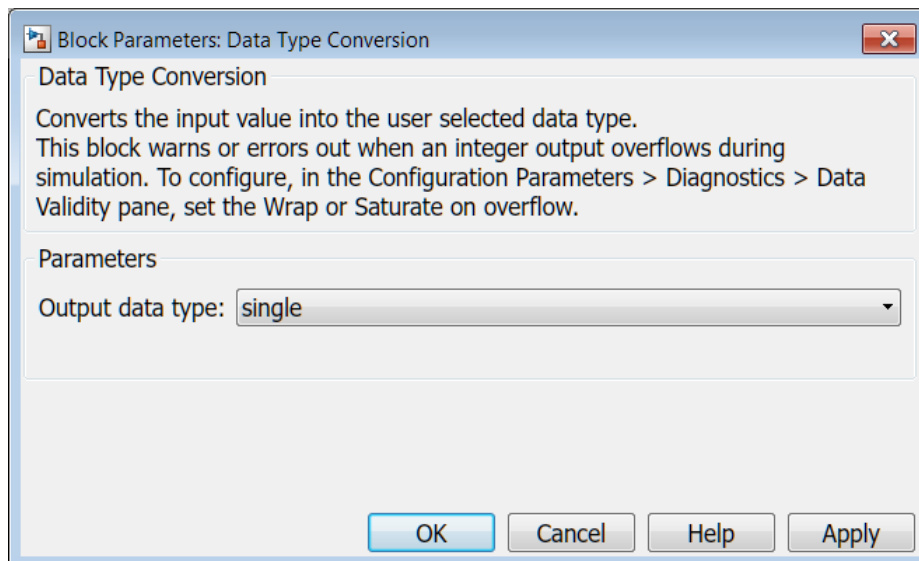
**Figure 8: RGB to YCbCr Subsystem with DTC Blocks Connected**

4. Open the **Data Type Conversion** blocks at the inputs of the **RGB to YCbCr** Subsystem, and do the following:
  - Change the **Output data type** parameter to **fixed**.
  - Set the **Signedness** to **Unsigned**.
  - Set the **Word length** to **8**.
  - Set **Fractional length** to **7**.
  - Click **Apply**, and close the dialog box.



**Figure 9: Data Type Conversion Block Parameters**

5. Add the **Data Type Conversion** blocks at the output of the **RGB to YCbCr** Subsystem and set the **Output data type** parameter to **single**. This will enable connecting the output signals to the Video Viewer blocks for visualization.



**Figure 10: Setting Output Data Type**

6. Double-click the **RGB to YCbCr** subsystem to descend the hierarchy and open the model. Within the **RGB to YCbCr** subsystem, there are subsystems to calculate Y, Cb, and Cr components using Gain and Constant blocks.

You can control the fixed point types for the gain parameter in the **Gain** blocks and the value in the **Constant** blocks. You can do this by opening up the **Calculate\_Y**, **Calculate\_Cb**, and **Calculate\_Cr** blocks and setting the data types as follows.

For **Gain** blocks, set the **Gain data type** to **fixed** and the following options appear:

- **Signedness** to **Signed**
- **Gain data type** to **fixed**
- **Word length** to **8**
- **Fractional length** to **7**

For **Constant** blocks, on the **Data Types** tab set the **Output data type** to **fixed** and the following options appear:

- **Signedness** to **Signed**
- **Output data type** to **fixed**
- **Word Length** to **8**
- **Fractional Length** to **7**

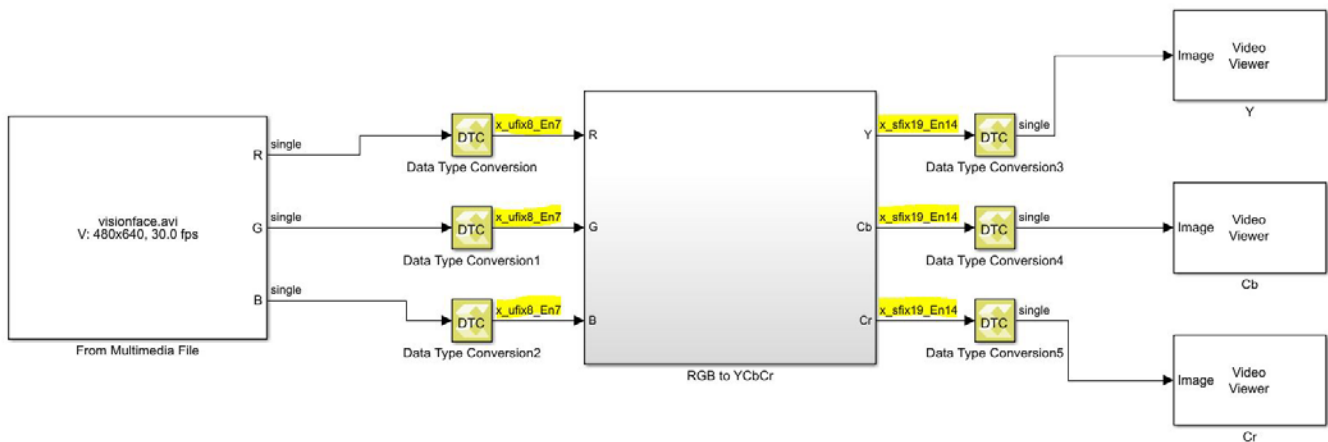



---

**TIP:** You can use the **View > Property Inspector** command to open the *Property Inspector* window. When you select the different Gain or Constant blocks, you can see and modify the properties on the selected block.

---

Make sure you do this for all the Constant and Gain blocks in the design. Update the model (**Ctrl+D**) and observe the fixed point data types being propagated along with automatic bit growth in gain blocks and adder trees in the design as shown below:



**Figure 11: Propagated Xilinx Fixed-Point Data Types**

The general format used to display the Xilinx fixed point data types is as follows:

**x\_[u/s]fix[wl]\_En[fl]**

**u:** Unsigned

**s:** Signed

**wl:** Word Length

**fl:** Fractional Length

For example, **x\_sfix16\_En8** represents a signed fixed point number with Word Length=16 and Fractional Length=8.

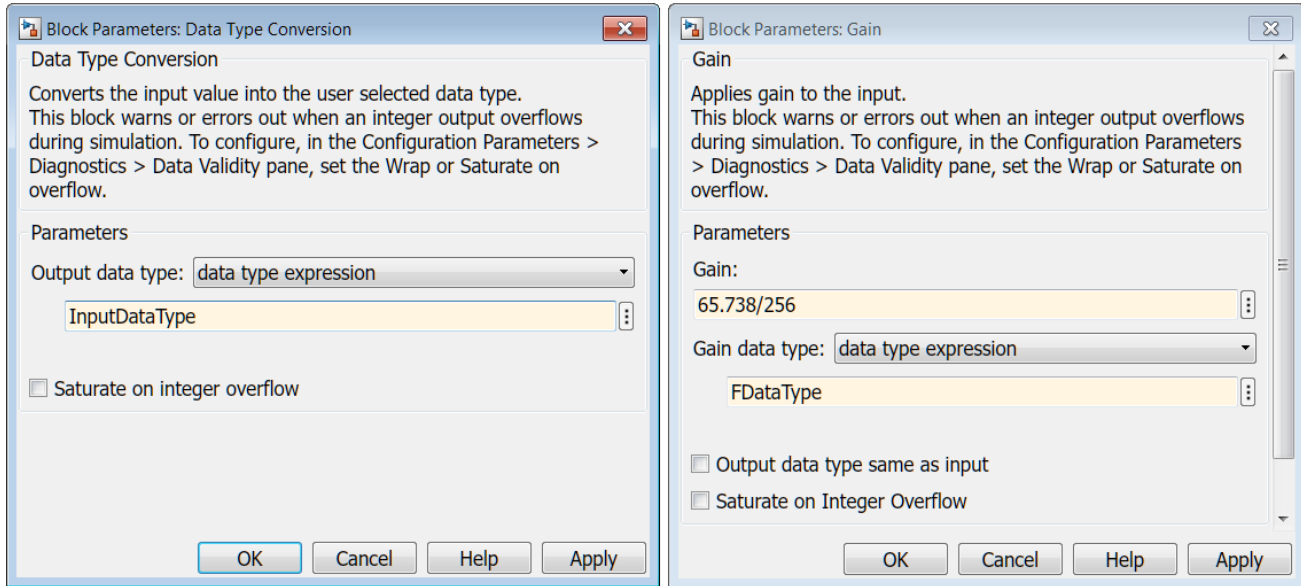
You can view a completed version of the design here:

ModelComposer\_Tutorial\Lab1\Section2\solution\Colorspace\_Conversion\_fixed .slx

### **Convert Data Types (Alternative)**

Model Composer supports Data Type Expressions that make it easier to change data types and quickly explore the results from your design.

1. Double-click `ColorSpace_Conversion_Expression.slx` in the Current Folder to open the design.
2. Notice that the **Data Type Conversion** blocks at the Input of the **RGB to YCbCr** Subsystem, the **Gain** blocks and **Constant** blocks within the Subsystem have corresponding **Output data type** and **Gain data type** set to **data type expression**.



**Figure 12: Controlling Data Types with Workspace Variables**

This enables Model Composer blocks to control the data types in the design using workspace variables, in this case `InputDataType` and `FDataType` that you can easily change from the MATLAB command prompt.

- Update the model (**Ctrl+D**) and observe the fixed-point data types propagated through the blocks. The other Model Composer blocks in the design will automatically take care of the bit-growth in the design. If you want more control over the fixed point data types at other intermediate portions of the design, you can insert **Data Type Conversion** blocks wherever necessary.

- To change the fixed point types in the **Gain** and **Constant** blocks, type the following at the MATLAB command prompt:

```
>> FDataType = 'x_sfix8_En6'
>> InputDataType = 'x_ufix8_En6'
```

'**x\_sfix8\_En6**' represents a signed fixed point number with Word Length 8 and Fractional Length 6.

Now update the model (**Ctrl+D**) and observe how the fixed-point data types have changed in the design.

- Simulate the model and observe the results from the design. Try further changing **InpuDataType** and **FDataType** variables through command line and iterate through multiple word lengths and fractional lengths. See the Additional Details section below for information on specifying rounding and overflow modes.

### **Additional Details:**

In the example above, we only specified the Word Length and Fractional Length of the fixed point data types using data type expressions. However, for greater control over the fixed point types in your

design, you can also specify the Signedness, Rounding, and Overflow. In general the format used for specifying fixed point data types using the data type expression is

**x\_[u/s]fix[wl]\_En[fl]\_[r<round>w<overflow>]**

**u:** Unsigned

**s:** Signed

**wl:** word length

**fl:** Fractional length

**<round>:** Specify the corresponding index from table below. It's optional. If not specified, default value is 6 (Truncation to minus infinity). Note that for the rounding cases (1 to 5), the data is rounded to the nearest value that can be represented in the format. When there is a need for tie breaker, these particular roundings behave as specified in the **Meaning** column.

Index	Meaning
1	Round to Plus Infinity
2	Round to Zero
3	Round to Minus Infinity
4	Round to Infinity
5	Convergent Rounding
6	Truncation to Minus Infinity
7	Truncation to Zero

**<overflow>:** Specify the corresponding index from table below. It's optional. If not specified, default value is 4 (Wrap around)

Index	Meaning
1	Saturation
2	Saturation to Zero
3	Symmetrical Saturation
4	Wrap Around
5	Sign-Magnitude Wrap Around

**Example.** `x_ufix8_En6_r6w4` represents a fixed point data type with

**Signedness:** Unsigned

**Word Length:** 8

**Fractional Length:** 6

**Rounding Mode:** Truncation to Minus Infinity

**Overflow Mode:** Wrap Around

## Conclusion

In this lab, you learned:

- How to connect Model Composer blocks directly to native Simulink blocks.
- How the Model Composer blocks *support Vectors and Matrices*, allowing you to process an entire frame of an image at a time without converting it from a frame to a stream of pixels at the input.
- How to work with different data types.
- How to use the Data Type Conversion block to control the conversion between data types, including floating-point to fixed-point data types.

*Note: Model Composer Supports the same floating and integer data types as Simulink blocks. Model Composer also supports Xilinx fixed point data types.*

The following `solution` directories contain the final Model Composer files for this lab:

`C:\ModelComposer_Tutorial\Lab1\Section1\solution`

`C:\ModelComposer_Tutorial\Lab1\Section2\solution`

---

### Introduction

Model Composer lets you import Vivado HLS library functions and user C/C++ code as custom blocks to use in your algorithm for both simulation and code generation.

The Library Import feature is a MATLAB function, `xmcImportFunction`, which lets you specify the required source files and automatically creates an associated block that can be added into a model in Simulink.

This lab primarily have two parts

- In Step 1, you are introduced to the `xmcImportFunction` function, and walk through an example.
- In Step 2, you will learn about the Model Composer feature that enables you to create custom blocks with function templates

For more details and information about other Model Composer features, see the Model Composer User Guide ([UG1262](#)).

---

### Step 1: Set up the Import Function Example

In the MATLAB `Current Folder` panel, navigate to `Lab2\Section1` folder.

7. Double-click the `basic_array.cpp` and `basic_array.h` files to view the source code in the MATLAB Editor.

These are the source files for a simple `basic_array` function in C++, which calculates the sum of two arrays of size 4. You will import this function as a Model Composer block using the `xmcImportFunction` function.

The input and output ports for the generated block are determined by the signature of the source function. Model Composer identifies arguments specified with the `const` qualifier as inputs to the block, and all other arguments as outputs.

**Note:** For more details and other options for specifying the direction of the arguments, see the Model Composer User Guide ([UG1262](#)).



---

**IMPORTANT:** You can use the `const` qualifier in the function signature to identify the inputs to the block or use the pragma `IMPORT`.

---

In the case of the `basic_array` function, the `in1` and `in2` arguments are identified as inputs.

```
void basic_array(
    uint8_t out1[4],
    const uint8_t in1[4],
    const uint8_t in2[4])
```

8. To learn how to use the `xmcImportFunction` function, type `help xmcImportFunction` at the MATLAB command prompt to view the help text and understand the function signature.
9. Open the `import_function.m` MATLAB script, and fill in the required fields for the `xmcImportFunction` function in this way:

```
xmcImportFunction('basic_array_library', {'basic_array'}, 'basic_array.h',
    {'basic_array.cpp'}, {});
```

The information is defined as follows:

- **Library Name:** `basic_array_library`. This is the name of the Simulink library that is created with the new block.
- **Function Names:** `basic_array`. This is the name of the function that you want to import as a block.
- **Header File:** `basic_array.h`. This is the header file for the function.
- **Source Files:** `basic_array.cpp`. This is the source file for the imported function.
- **Search Paths:** This argument is used to specify the search path(s) for header files. In this example, there are no additional search paths to specify and hence you can leave it as `{ }` which indicates none.

*Note: Look at `create_library_solution.m` in the `solution` folder for the completed version.*

10. Run the `import_function.m` script from the MATLAB command line:

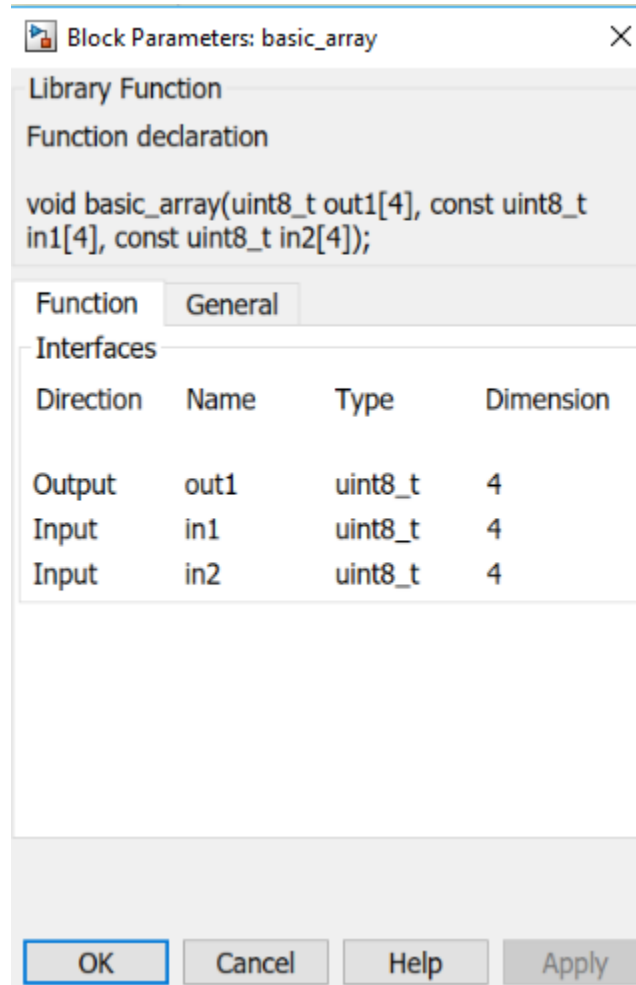
```
>>run('import_function.m')
```

Notice that a Simulink library model opens up with the generated block `basic_array`.

Save this Simulink library model.

11. Double-click the **`basic_array`** block, and look at the generated interface.

The following figure shows the Block Parameters dialog box for **`basic_array`**:



**Figure 13: Block Parameters: basic\_array Block**

12. Open the `test_array.slx` model, which is just a skeleton to test the generated block.
13. Add the generated **basic\_array** block into this model, then connect the source and sink blocks.
14. Simulate this model and observe the results in the display block.

## Step 2: Custom Blocks with Function Templates

In this step we will walk through an example to do the following:

- To create a custom block that supports inputs of different sizes.
- To create a custom block that accepts signals with different fixed-point lengths and fractional lengths.
- To perform simple arithmetic operations using template variables.

1. Navigate to the Lab2/section2 folder
2. Double click the template\_design.h file to view the source code in the MATLAB Editor. There are two functions: Demux and Mux. These two functions are a multiplexing and demultiplexing of inputs as shown below.

```
#pragma XMC INPORT vector_in
template<int NUMOFELEMENTS, int W, int I>
void Demux(ap_fixed<W,I> vector_in[NUMOFELEMENTS], ap_fixed<W,I> vector_out0[NUMOFELEMENTS/2],
          ap_fixed<W,I> vector_out1[NUMOFELEMENTS/2]) {
    for (int i = 0; i < NUMOFELEMENTS/2; i++) {
        vector_out0[i] = vector_in[i];
        vector_out1[i] = vector_in[i+NUMOFELEMENTS/2];
    }
}
```

Figure 14: Demux Function

3. In the piece of code, note the `#pragma XMC INPORT vector_in`. This is a way to manually specify port directions using pragmas. Here, we are specifying the function argument `vector_in` as the InputPort. Similarly, we can define XMC OUTPORT also.

**Note:** For additional information about specifying ports, see *Importing C/C++ Code as Custom Blocks in the Model Composer User Guide (UG1262)*.

4. Notice the use of `template` before the function declaration. To support the inputs of different sizes, `NUMOFELEMENTS` is declared as a parameter and used the same while defining an array `vector_in` as shown below. This allows you to connect signals of different sizes to the input port of the block.

```
template<int NUMOFELEMENTS, int W, int I>
void Demux(ap_fixed<W,I> vector_in[NUMOFELEMENTS], ap_fixed<W,I> vector_out0[NUMOFELEMENTS/2],
          ap_fixed<W,I> vector_out1[NUMOFELEMENTS/2]) {
```

5. Notice the template parameters  $W$  and  $I$  which are declared to accept signals with different word lengths and integer lengths.

```
template<int NUMOFELEMENTS, int W, int I>
void Demux(ap_fixed<W,I> vector_in[NUMOFELEMENTS], ap_fixed<W,I> vector_out0[NUMOFELEMENTS/2],
          ap_fixed<W,I> vector_out1[NUMOFELEMENTS/2]) {
```

**Note:** The same library is specified for both the functions.

6. Observe the arithmetic operations performed using template variables as shown below, indicating the output signal length is half of the input signal length.

```
void Demux(ap_fixed<W,I> vector_in[NUMOFELEMENTS], ap_fixed<W,I> vector_out0[NUMOFELEMENTS/2],
          ap_fixed<W,I> vector_out1[NUMOFELEMENTS/2]) {
```

7. Similar explanation follows for Mux function.

```
#pragma XMC INPORT vector_in0
#pragma XMC INPORT vector_in1
template<int NUMOFELEMENTS, int W, int I>
void Mux(ap_fixed<W,I> vector_in0[NUMOFELEMENTS], ap_fixed<W,I> vector_in1[NUMOFELEMENTS],
        ap_fixed<W,I> vector_out[NUMOFELEMENTS*2]) {
    for (int i = 0; i < NUMOFELEMENTS; i++) {
        vector_out[i] = vector_in0[i];
        vector_out[i+NUMOFELEMENTS] = vector_in1[i];
    }
}
```

Figure 15: Mux Function

Now create the library blocks for Mux and Demux functions using the `xmcImportFunction` command and complete the design below with custom blocks.

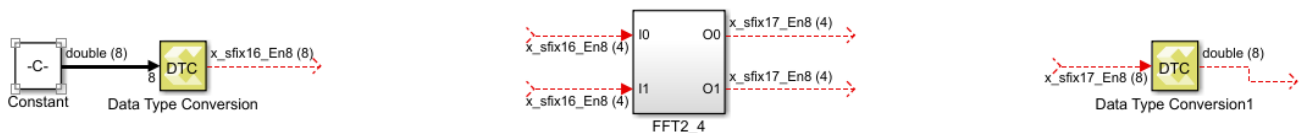


Figure 16: Initial Design

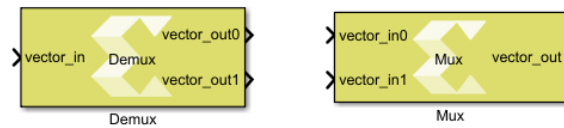
8. Double-click the `import_function.m` script file in the MATLAB command window and observe the following commands that generate library blocks to embed into your actual design.

```
>>xmcImportFunction('design_lib', {'Demux'}, 'template_design.h', {}, {'$XILINX_VIVADO_HLS/include'}, 'override', 'unlock')
>>xmcImportFunction('design_lib', {'Mux'}, 'template_design.h', {}, {'$XILINX_VIVADO_HLS/include'}, 'override', 'unlock')
```

9. Run the `import_function.m` script from the MATLAB command line:

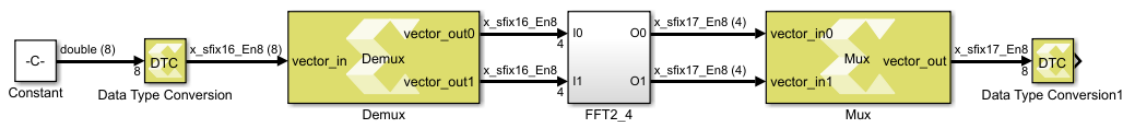
```
>>run('import_function.m')
```

10. Observe the generated library blocks in the `design_lib.slx` library model file and save it to working directory.



**Figure 17: Generated Library blocks**

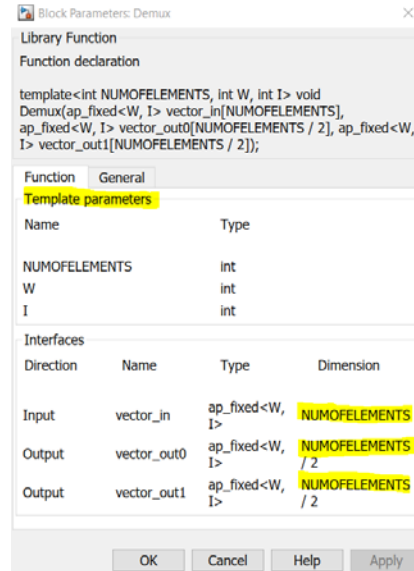
11. Copy the Demux and Mux blocks and paste them in the `design.slx` file and connect them as shown below.



**Figure 18: Completed Design**

12. Note the following after embedding the custom blocks:

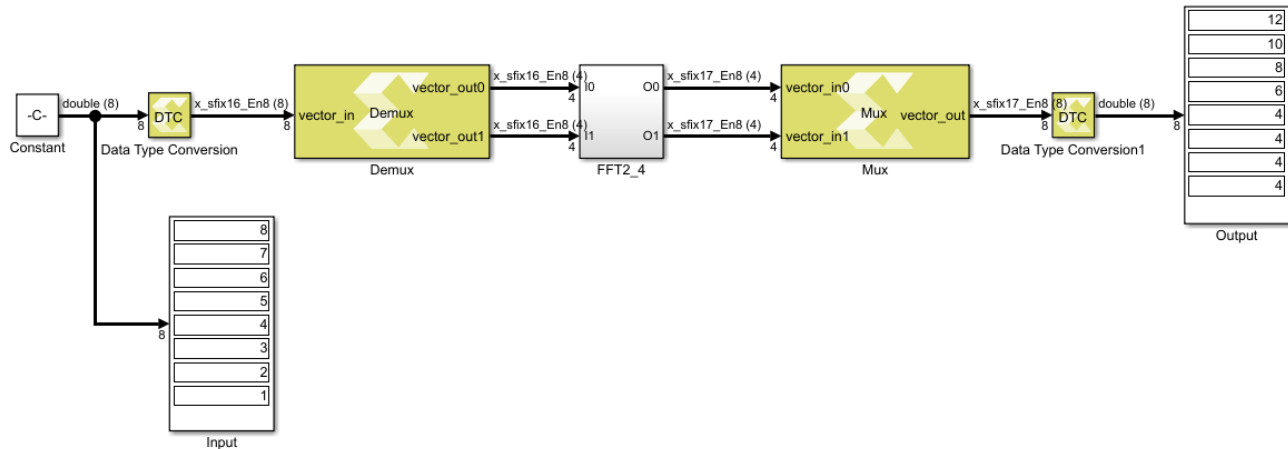
- a. Double-click the Constant block and observe the vector input of type `double`. `SSR` is a workspace variable, initially set to **8** from the `initFcn` model callback.
- b. Using the Data Type Conversion (DTC) block, `double` type is converted to `fixed` type with 16-bit word length and 8-bit fractional length.  
Input is configurable to any word length since the design is templated.
- c. Double-click the Demux block and observe the **Template parameters** section and **Dimension** column in the Interface section of the function tab.



**Figure 19: Library Function Block Parameters**

d. Next, double-click the Mux block and observe the **Template parameters** and **Dimension**.

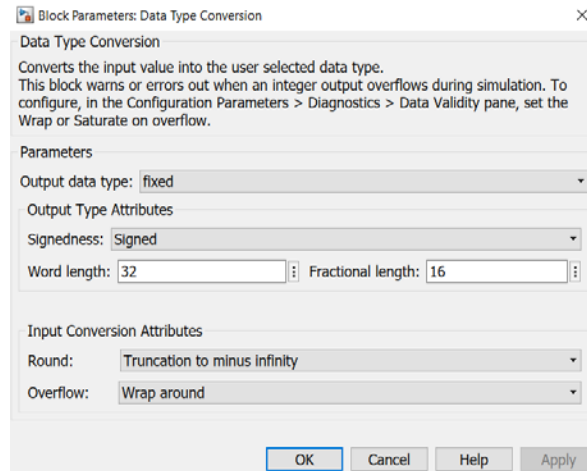
13. Add a Display block at the input and output as shown below and simulate the model to observe the results.



**Figure 20: Output after Simulation**

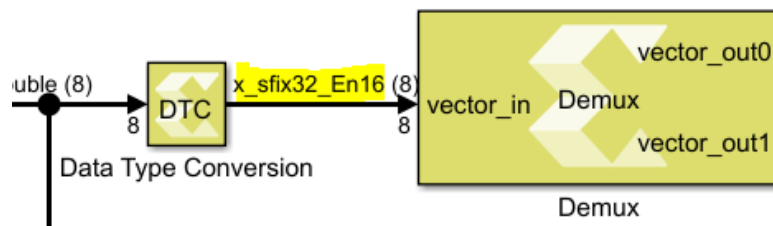
14. To understand how templated inputs add advantage and flexibility to your design, perform the following:

- Double-click the DTC block.
- In the Block Parameters dialog box, change the **Word length** from 16 to 32.
- Change the **Fractional length** from 8 to 16.



**Figure 21: DTC Block Parameters**

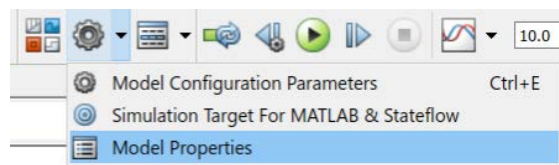
- d. Click **OK** and press Ctrl+D. Observe the signal dimensions in the design.



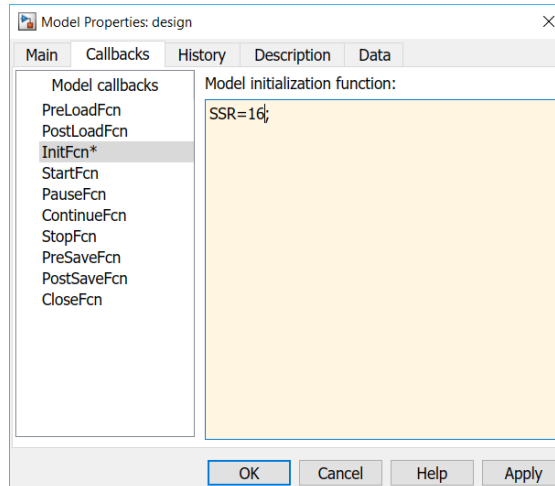
**Figure 22: Signal Dimensions in Design**

To make sure the output is correct, run the simulation and observe that the same block can still be used in a generic way for different values of Word length and Fractional length. This is possible only because we have templated the  $w$  and  $I$  values in our C design.

- 15. For an additional understanding of template parameters, perform the following:
  - a. Click the arrow mark beside the **Model configuration Parameters** icon and select the **Model Properties** option.

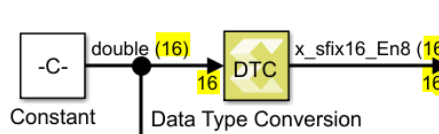


- b. In the Model Properties window, go to the Callbacks tab and select **initFcn** and edit the **SSR** value from **8** to **16** as shown below.



**Figure 23: Model Properties**

- c. Click **OK** and press Ctrl+D to observe the change in the number of elements in the Constant block output vector. The bitwidth changes when we change the datatype on the input DTC. This is possible only because of the template parameter NUMOFELEMENTS.



- d. Run the simulation and validate the output according to the input values.

**Note:** For information about features such as function templates for data types and pragmas to specify which data type a template variable supports, see *Defining Blocks Using Function Templates in the Model Composer User Guide (UG1262)*.

## Conclusion

In this lab, you learned:

- How to create a custom block using the `xmcImportFunction` in Model Composer.
- How to create a block that accepts signals with different fixed-point lengths and fractional lengths.
- How to use the syntax for using a function template that lets you create a block that accepts a variable signal size or data dimensions.
- How to perform simple arithmetic operations using template variables.

*Note: Current feature support enables you to import code that uses:*

- *Vectors and 2D matrices*
- *Floating, integer, and Vivado HLS fixed-point data types*

The following `solution` directory contains the final Model Composer (\*.slx) files for this lab.

`C:\ModelComposer_Tutorial\Lab2\section1\solution`

`C:\ModelComposer_Tutorial\Lab2\section2\solution`

---

### Introduction

In this lab, you look at the flow for generating output from your Model Composer model and moving it into downstream tools like Vivado HLS for RTL synthesis, or into System Generator, or the Vivado Design Suite for implementation into a Xilinx device.

### Procedure

This lab has five steps:

In Step 1, you will review the requirements for automatic code generation.

In Step 2, you will look at how to map Interfaces in your design.

In Step 3, you will look at the flow for generating an IP from your Model Composer design.

In Step 4, you will look at the flow for generating HLS Synthesizable C++ code from the Model Composer design.

In Step 5, you will look at the flow to port a Model Composer design back into System Generator for DSP as a block.

---

### Step 1: Review Requirements for Generating Code

In this step, you review the three requirements to move from your algorithm in Simulink to an implementation through automatic code generation.

1. In the MATLAB `Current Folder`, navigate to the `ModelComposer_Tutorial\Lab3` directory.
2. Double-click `CodeGen_start.slx` to open the model.

To prepare for code generation, you will enclose your Model Composer design in a subsystem.

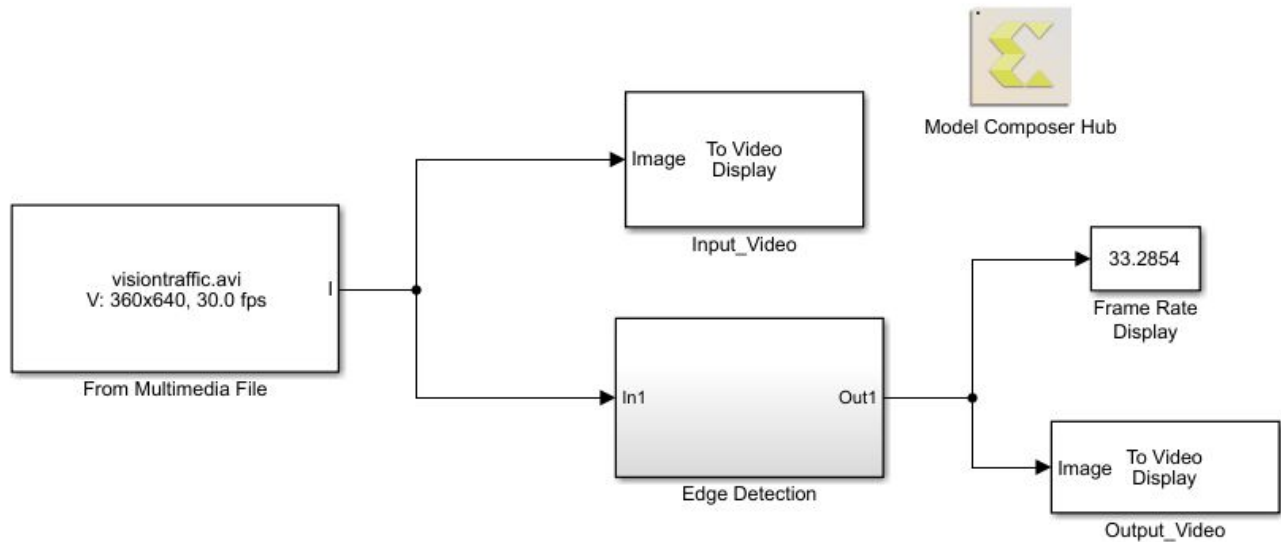
3. Right-click the **Edge Detection** area, and select **Create Subsystem from Area**.

*Note: For code generation to work, all the blocks within the enclosed subsystem should only be from the Xilinx Model Composer library, with the exception of the Simulink blocks noted below. Subsystems with unsupported blocks will generate errors during code generation. The Simulink diagnostic viewer will contain error messages and links to the unsupported blocks in the subsystem.*

**Note:** In addition to the base Model Composer blocks, a subset of native Simulink blocks such as From, Goto, Bus Creator, Bus Selector, If, and others, are supported. The supported Simulink blocks appear within the Xilinx Model Composer libraries as well.

Next, you add the **Model Composer Hub** block at the top level of your design.

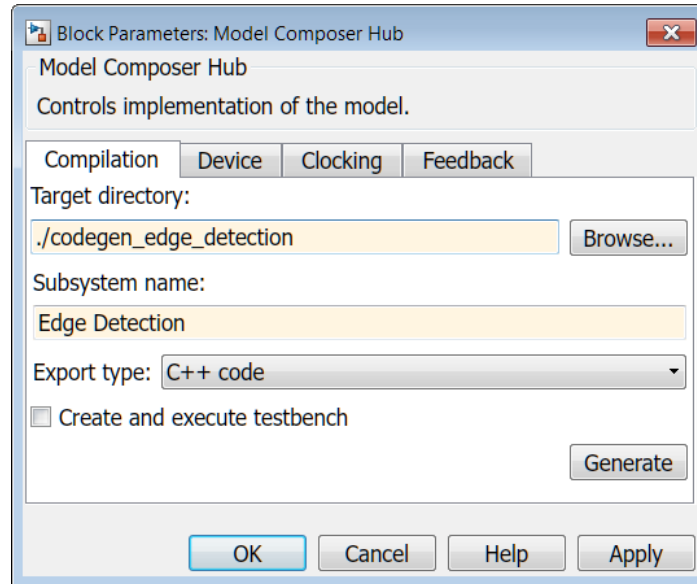
4. Open the Simulink Library Browser and navigate to **Xilinx Model Composer Tools** sub-library.
5. Find the **Model Composer Hub** block, and add it into the design as shown in the following figure:



**Figure 24: Edge Detection with Model Composer Hub Block**

Next, you use the **Model Composer Hub** block to select the code generation options for the design.

6. Double-click the block to open the block interface and set up as shown in the following figure:



**Figure 25: Block Parameters Dialog Box**

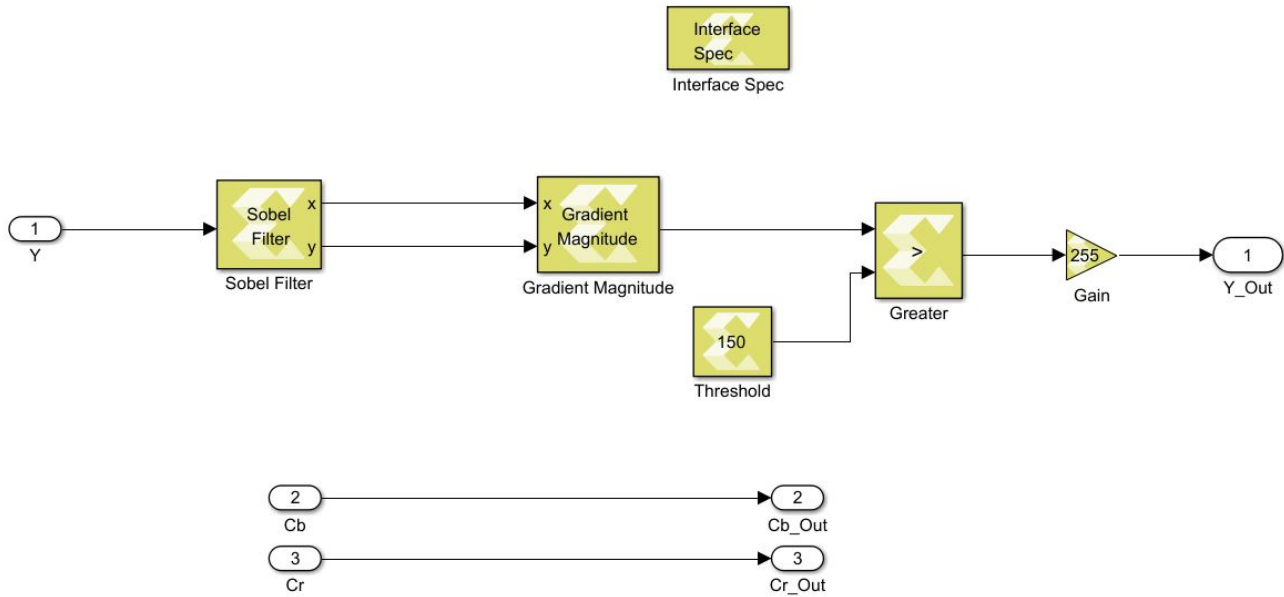
7. On the Compilation tab, you can select the following:
  - **Target Directory:** Location for the generated code
  - **Subsystem name:** In this case, the **Edge Detection** subsystem. You can have multiple subsystems at the top-level and use the **Model Composer Hub** block to select and individually compile the subsystem you want.
  - **Export Type:** This option determines what you want to convert your design into.
    - (1) IP Catalog (*default*)
    - (2) Vivado HLS Synthesizable C++ code
    - (3) System Generator for DSP
8. On the Clocking tab, you can specify the target **FPGA clock frequency** in MHz. The default value is 200MHz.

---

## Step 2: Mapping Interfaces

1. Double-click the `CodeGen_Interface.slx` model in your Current Folder to open the design for this lab section.
 

This is a slightly modified version of the Edge Detection algorithm that uses the YCbCr video format at the input and output.
2. Simulate the model to see the results in the **Video Viewer** blocks.
3. Open the Simulink Library browser, navigate to the Xilinx **Model Composer > Tools** sub-library and add the **Interface Spec** block inside the **Edge Detection** subsystem as shown in the following figure:

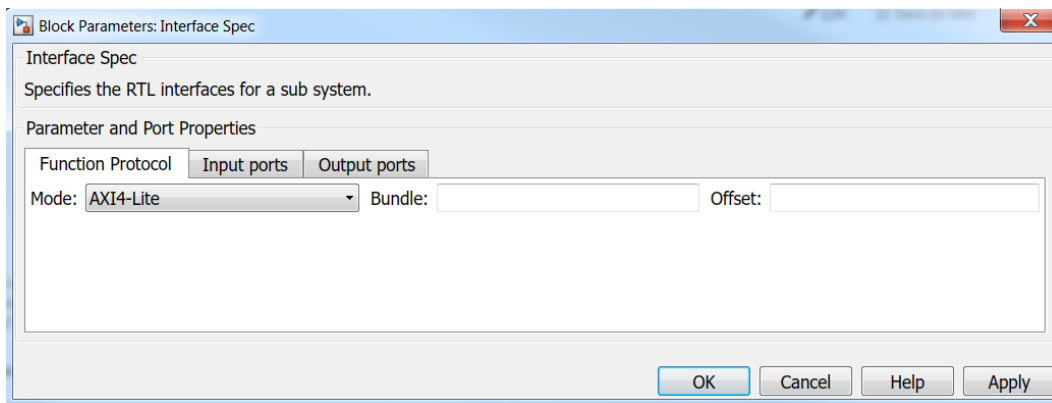


**Figure 26: Interface Spec Block**

4. Double-click the **Interface Spec** block to open the block interface.

The **Interface Spec** block allows you to control what RTL interfaces should be synthesized for the ports of the subsystem in which the block is instantiated. This affects only code generation; it has no effect on Simulink simulation of your design.

The information gathered by the Interface Spec block consists of three parts (represented as three Tabs on the block):



**Figure 27: Interface Spec Block Parameter**

- **Function Protocol:** This is the block-level Interface Protocol which tells the IP when to start processing data. It is also used by the IP to indicate whether it accepts new data, or whether it has completed an operation, or whether it is idle.
- **Input Ports:** Detects the Input ports in your subsystem automatically and allows specifying the port-level Interface Protocol for each input port of the subsystem.

- **Output Ports:** Similar to the Input Ports tab, this tab detects the Output ports in the subsystem, and allows specifying the port-level Interface Protocol for each output port of the subsystem.
5. For this design, leave the **Function Protocol** mode at the default **AXI4-Lite** and configure the Input ports and Output ports tabs as shown in the following figures:

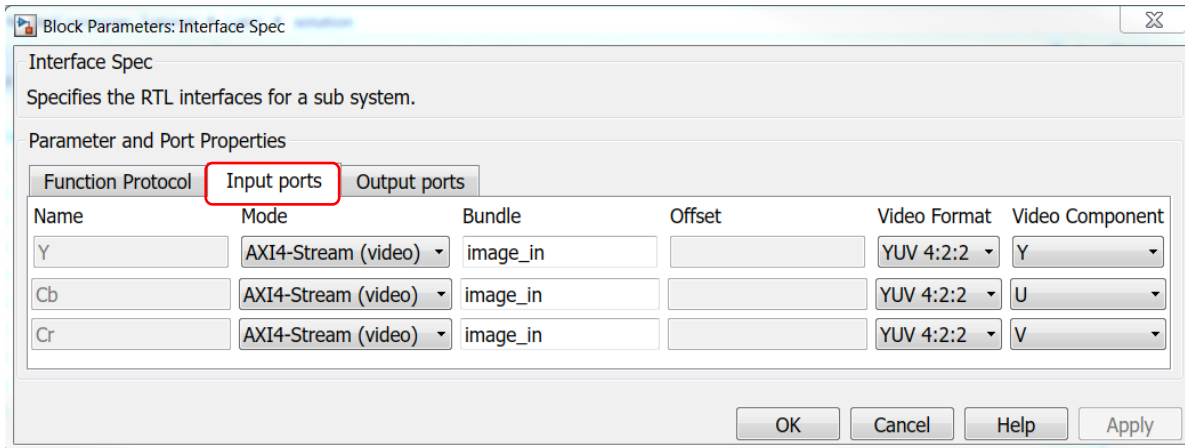


Figure 28: Input Port Settings

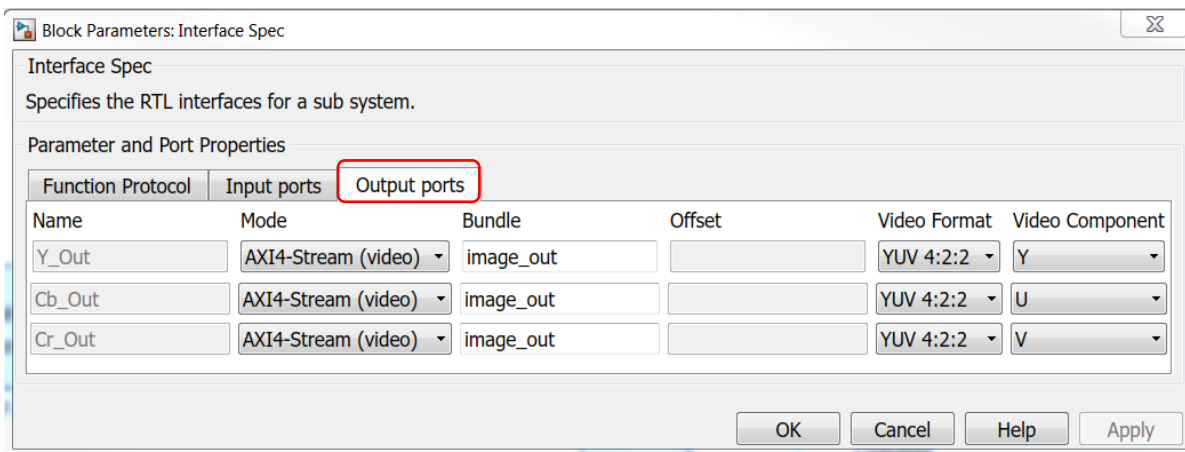


Figure 29: Output Port Settings

- The **Bundle** parameter is used in conjunction with the AXI4-Lite or AXI4-Stream (video) interfaces to indicate that multiple ports should be grouped into the same interface. It lets you bundle multiple input/output signals with the same specified bundle name into a single interface port and assigns the corresponding name to the RTL port.

For example in this case, the specified settings on the Input ports tab result in the YCbCr inputs being mapped to AXI4-Stream (video) interfaces and bundled together as an `image_in` port in the generated IP while the YCbCr outputs are bundled together as an `image_out` port.

- The **Video Format** drop-down menu lets you select between the following formats:
  - **YUV 4:2:2**
  - **YUV 4:4:4**

- **RGB**
- **Mono/Sensor**
- The **Video Component** drop-down menu is used to subsequently select the right component: R,G,B,Y,U,V.

---

## Step 3: Generate IP from Model Composer Design

Using the same example, you will generate an IP from the Edge Detection algorithm.

1. Double-click the `CodeGen_IP.slx` model in the Current Folder.
2. Double-click the **Model Composer Hub** block, and set the following in the block dialog box:
  - **Export Type: IP Catalog (default)**
  - **Target Directory:** `codegen_IP`
  - **Subsystem name:** `Edge Detection`
3. In the `CodeGen_IP.slx` model, double-click into the **Edge Detection** subsystem and review the settings on the **Interface Spec** block. Based on the previous lab, this block has already been set up to map the input and output ports to AXI4-Stream Video interface and to use the YUV 4:2:2 video format.
4. To generate an IP from this design, click the **Apply** button in the **Model Composer Hub** block dialog box to save the settings. Then click the **Generate** button to start the code generation process.

Model Composer opens a progress window to show you the status. After completion, click **OK** and you will see the new `codegen_IP` folder in the current folder, which contains the generated IP `solution` folder.

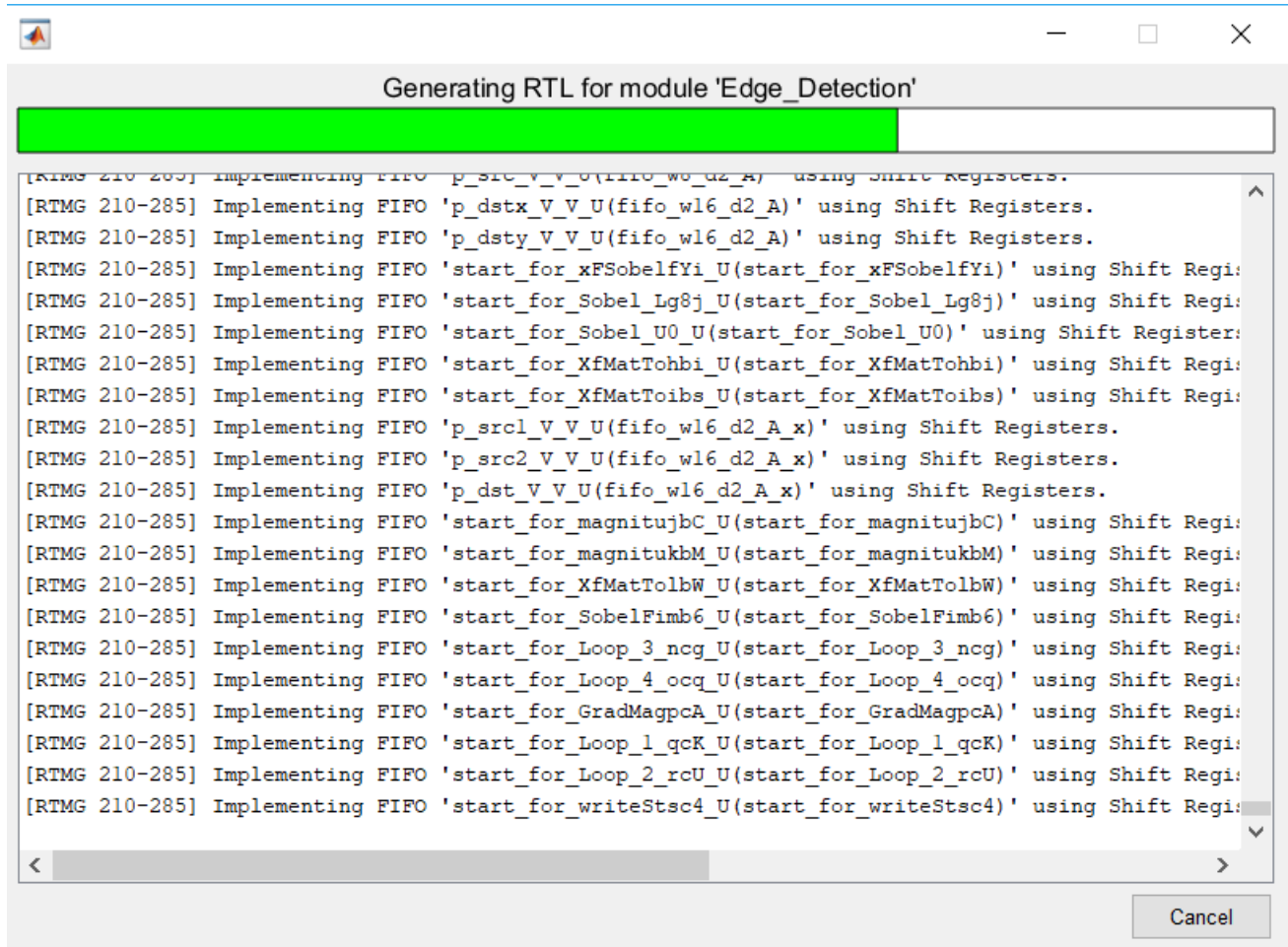


Figure 30: Generation Progress

At the end of the IP generation process, Model Composer opens the **Performance Estimates** and **Utilization Estimates** (from Vivado HLS Synthesis report) in the MATLAB Editor, as shown in the following figures:

**Note:** The Performance and Utilization Numbers here may vary slightly depending on software release.

```

=====
== Performance Estimates
=====
+ Timing (ns):
  * Summary:
  +-----+-----+-----+-----+
  | Clock | Target| Estimated| Uncertainty|
  +-----+-----+-----+-----+
  | lap_clk | 5.00| 4.03| 0.63|
  +-----+-----+-----+-----+

+ Latency (clock cycles):
  * Summary:
  +-----+-----+-----+-----+
  | Latency | Interval | Pipeline |
  | min | max | min | max | Type |
  +-----+-----+-----+-----+
  | 464048| 464048| 234284| 234284| dataflow |
  +-----+-----+-----+-----+
    
```

**Figure 31: Performance Estimates**

```

=====
== Utilization Estimates
=====
* Summary:
+-----+-----+-----+-----+
| Name | BRAM_18K| DSP48E| FF | LUT |
+-----+-----+-----+-----+
| DSP | -| -| -| -|
| Expression | -| -| 0| 12|
| FIFO | 0| -| 0| 10|
| Instance | 12| -| 2562| 2994|
| Memory | -| -| -| -|
| Multiplexer | -| -| -| -|
| Register | -| -| -| -|
+-----+-----+-----+-----+
| Total | 12| 0| 2562| 3016|
+-----+-----+-----+-----+
| Available | 890| 840| 407600| 203800|
+-----+-----+-----+-----+
| Utilization (%) | 1| 0| ~0 | 1|
+-----+-----+-----+-----+
    
```

**Figure 32: Utilization Estimates**

You can also see a summary of the generated RTL ports and their associated protocols at the bottom of the report.

**Note :** *The actual timing and resource utilization estimates may deviate from above mentioned values, based on the Vivado HLS build you choose.*

```

=====
-- Interface
=====
* Summary:
-----
| RTL Ports | Dir | Bits | Protocol | Source Object | C Type |
-----
|s_axi_AXILites_AWVALID | in | 1 | s_axi | AXILites | return void |
|s_axi_AXILites_AWREADY | out | 1 | s_axi | AXILites | return void |
|s_axi_AXILites_AWADDR | in | 4 | s_axi | AXILites | return void |
|s_axi_AXILites_WVALID | in | 1 | s_axi | AXILites | return void |
|s_axi_AXILites_WREADY | out | 1 | s_axi | AXILites | return void |
|s_axi_AXILites_WDATA | in | 32 | s_axi | AXILites | return void |
|s_axi_AXILites_WSTRB | in | 4 | s_axi | AXILites | return void |
|s_axi_AXILites_ARVALID | in | 1 | s_axi | AXILites | return void |
|s_axi_AXILites_ARREADY | out | 1 | s_axi | AXILites | return void |
|s_axi_AXILites_ARADDR | in | 4 | s_axi | AXILites | return void |
|s_axi_AXILites_RVALID | out | 1 | s_axi | AXILites | return void |
|s_axi_AXILites_RREADY | in | 1 | s_axi | AXILites | return void |
|s_axi_AXILites_RDATA | out | 32 | s_axi | AXILites | return void |
|s_axi_AXILites_RRESP | out | 2 | s_axi | AXILites | return void |
|s_axi_AXILites_BVALID | out | 1 | s_axi | AXILites | return void |
|s_axi_AXILites_BREADY | in | 1 | s_axi | AXILites | return void |
|s_axi_AXILites_BRESP | out | 2 | s_axi | AXILites | return void |
|lap_clk | in | 1 | ap_ctrl_hs | Edge_Detection | return value |
|lap_rst_n | in | 1 | ap_ctrl_hs | Edge_Detection | return value |
|interrupt | out | 1 | ap_ctrl_hs | Edge_Detection | return value |
-----

|Y_TDATA | in | 16 | axis | image_in_V_data_V | pointer |
|Y_TKEEP | in | 2 | axis | image_in_V_keep_V | pointer |
|Y_TSTRB | in | 2 | axis | image_in_V_strb_V | pointer |
|Y_TUSER | in | 1 | axis | image_in_V_user_V | pointer |
|Y_TLAST | in | 1 | axis | image_in_V_last_V | pointer |
|Y_TID | in | 1 | axis | image_in_V_id_V | pointer |
|Y_TDEST | in | 1 | axis | image_in_V_dest_V | pointer |
|Y_TVALID | in | 1 | axis | image_in_V_dest_V | pointer |
|Y_TREADY | out | 1 | axis | image_in_V_dest_V | pointer |
|Y_Out_TDATA | out | 16 | axis | image_out_V_data_V | pointer |
|Y_Out_TKEEP | out | 2 | axis | image_out_V_keep_V | pointer |
|Y_Out_TSTRB | out | 2 | axis | image_out_V_strb_V | pointer |
|Y_Out_TUSER | out | 1 | axis | image_out_V_user_V | pointer |
|Y_Out_TLAST | out | 1 | axis | image_out_V_last_V | pointer |
|Y_Out_TID | out | 1 | axis | image_out_V_id_V | pointer |
|Y_Out_TDEST | out | 1 | axis | image_out_V_dest_V | pointer |
|Y_Out_TVALID | out | 1 | axis | image_out_V_dest_V | pointer |
|Y_Out_TREADY | in | 1 | axis | image_out_V_dest_V | pointer |
-----

```

Figure 33: Interface Summary

5. To add the generated IP to the Vivado IP catalog, *create a Vivado RTL project*.  
When you create the Vivado RTL project, specify the **Board** as **Kintex-7 KC705 Evaluation Platform** (which is the same as the default Board in the **Model Composer Hub** block).
6. In the **Vivado Flow Navigator**, click **IP Catalog**.
7. On the IP Catalog panel, select Vivado Repository, right-click and select **Add Repository**.
8. Select the `codegen_IP\Edge_Detection_prj\solution1\impl\ip` folder  
The generated **Edge\_detection** IP now shows in the IP catalog under **Vivado HLS IP**.

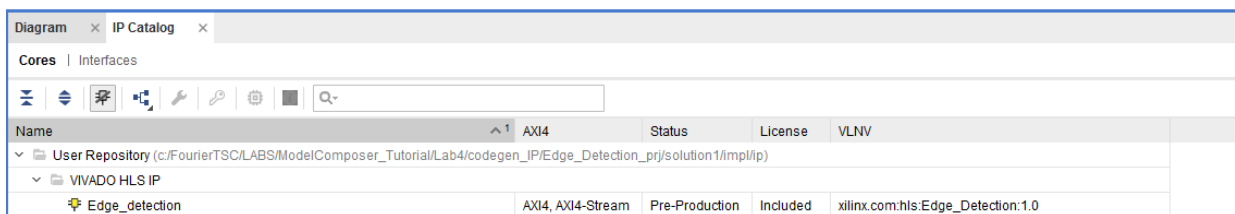


Figure 34: Edge\_detection IP in IP Catalog

You can now add this IP into an IP integrator block diagram, as shown in the following figure:

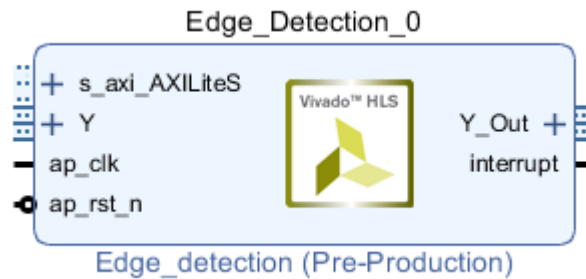


Figure 35: Edge\_Detection in IP Integrator

## Step 4: Generate HLS Synthesizable Code

In this section you will generate HLS Synthesizable code from the original Edge Detection design. Use the `CodeGen_Cplusplus.slx` design for this lab. Simulate the model and ensure that algorithm is functionally correct and gives you the results you would expect.

1. Open the **Model Composer Hub** block dialog box, and set the following:
  - o **Export Type:** C++ code
  - o **Target Directory:** ./codegen\_edge\_detection
  - o **Subsystem name:** Edge Detection
2. Click the **Apply** button on the **Model Composer Hub** block dialog box to save the settings and then click the **Generate** button to start the code generation process.

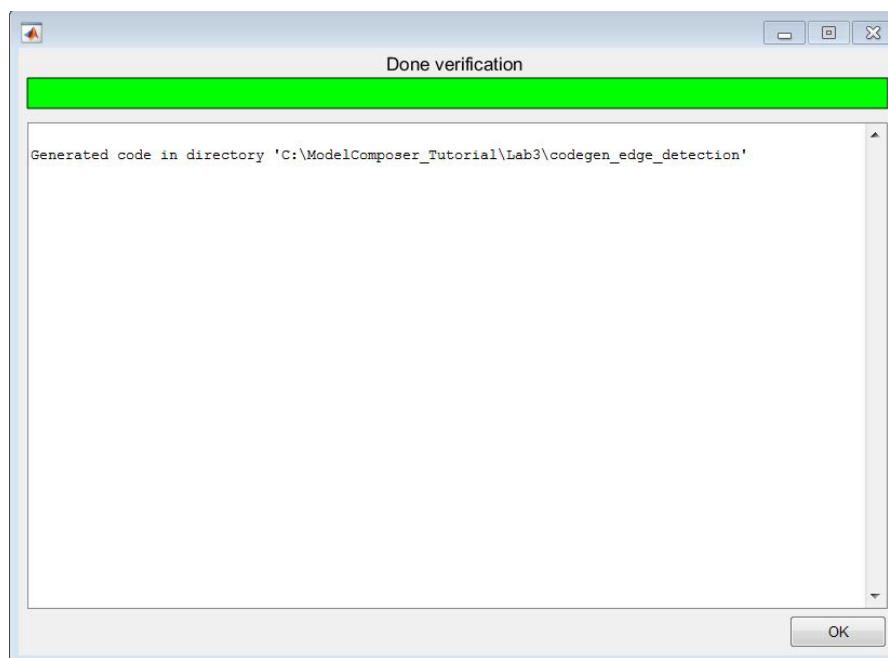


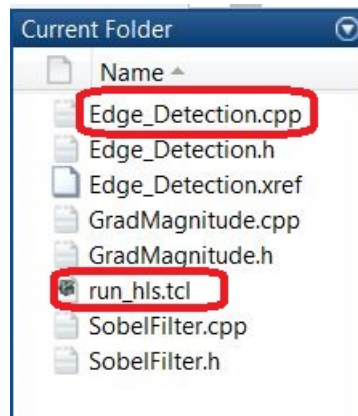
Figure 36: Code Generation Dialog Box

- At the end of code generation, observe the Current Folder in MATLAB.

You should now see a new folder: `codegen_edge_detection` in your Current Folder.

When you click **Generate** on the **Model Composer Hub** block, Model Composer first simulates the model, then generates the code and places the generated code files in the **Target Directory** folder. At the end of the code generation process, the window showing the progress of the code generation process tells you where to look for your generated code.

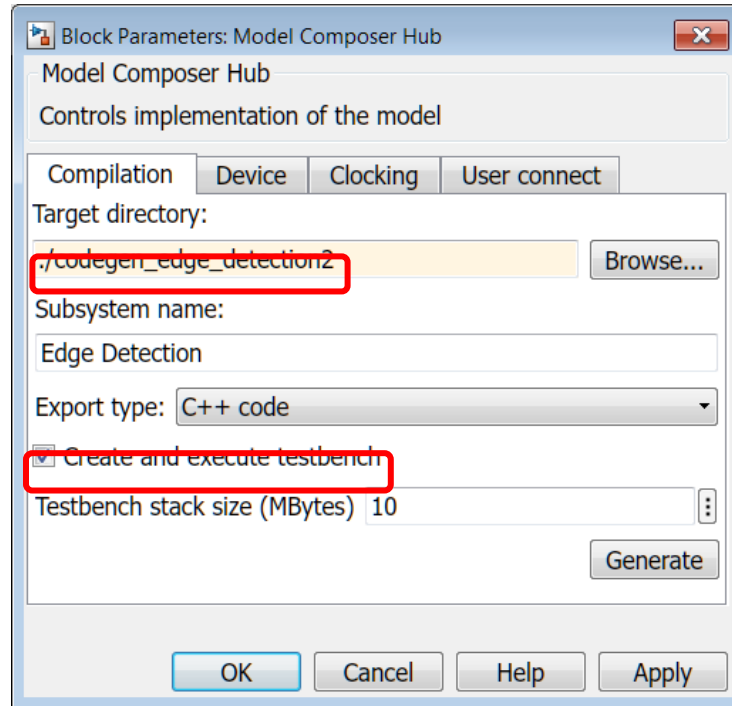
- Open the `codegen_edge_detection` folder and explore the generated code files highlighted in the following figure:



**Figure 37: Two Files to Explore in Current Folder**

**Note:**

- o `Edge_Detection.cpp` is the main file generated for the subsystem.
  - o `run_hls.tcl` is the Tcl file needed to create the Vivado HLS project and synthesize the design.
- In the design, open the **Model Composer Hub** block dialog box, and modify the block settings, shown in the following figure, as follows:
    - Check the **Create and execute testbench** checkbox.
    - Modify the **Target Directory** folder.

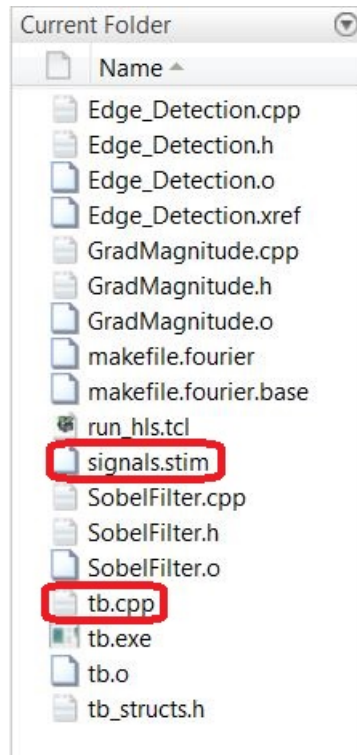


**Figure 38: Modify Parameters**

- Click **Apply** and regenerate the code by clicking the **Generate** button. Click OK after you see Done Verification in the status bar.

You should now see a new folder, `codegen_edge_detection2`, in your current folder.

- Open the `codegen_edge_detection2` folder and explore the generated code files.



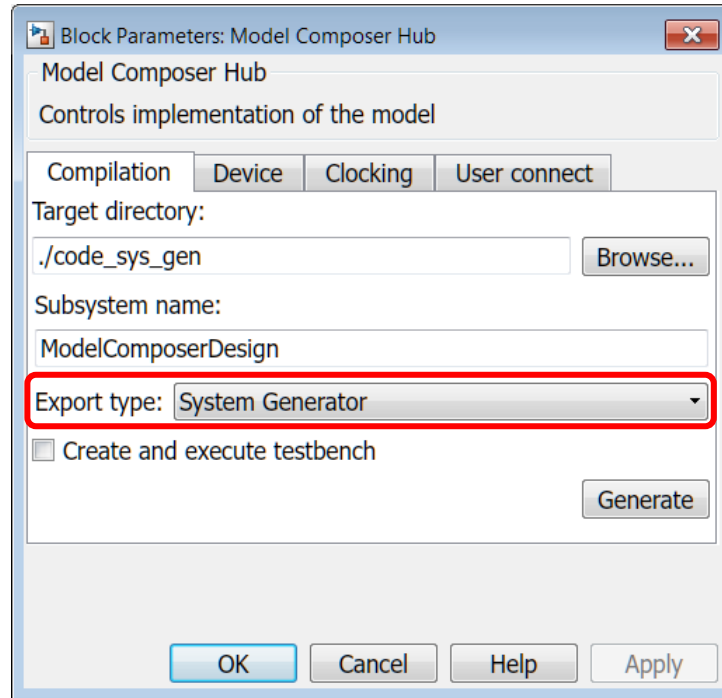
**Figure 39: codegen\_edge\_detection2 Folder**

With the **Create and execute testbench** option selected on the **Model Composer Hub** block, Model Composer logs the inputs and outputs at the boundary of the Edge Detection subsystem and saves the logged stimulus signals in the `signals.stim` file. The `tb.cpp` file is the automatically-generated test bench that you can use for verification in Vivado HLS. At the end of the code generation process, Model Composer automatically verifies that the output from the generated code matches the output logged from the simulation and reports any errors.

---

## Step 5: Port a Model Composer Design to System Generator

Using Model Composer, you can package a model for integration into a System Generator model, which is especially useful if you are an existing System Generator for DSP user. This allows you to take advantage of both the high level of abstraction and simulation speed provided by Model Composer for portions of your design, and the more architecture-aware environment provided by System Generator.

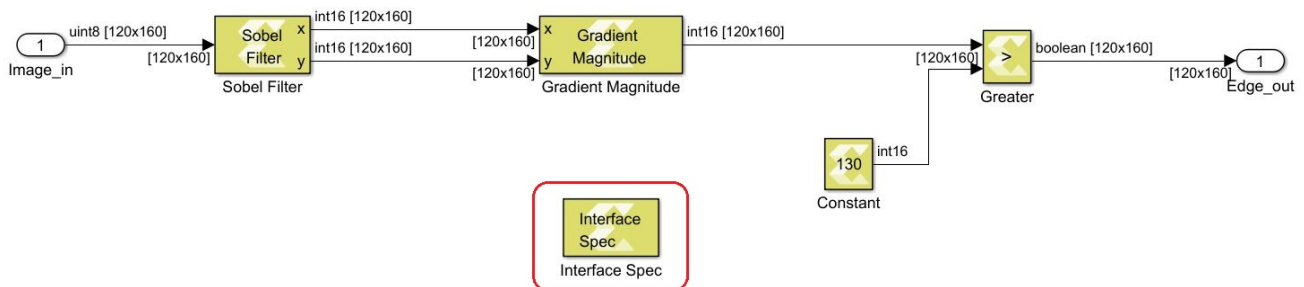


**Figure 40: System Generator Export Type**

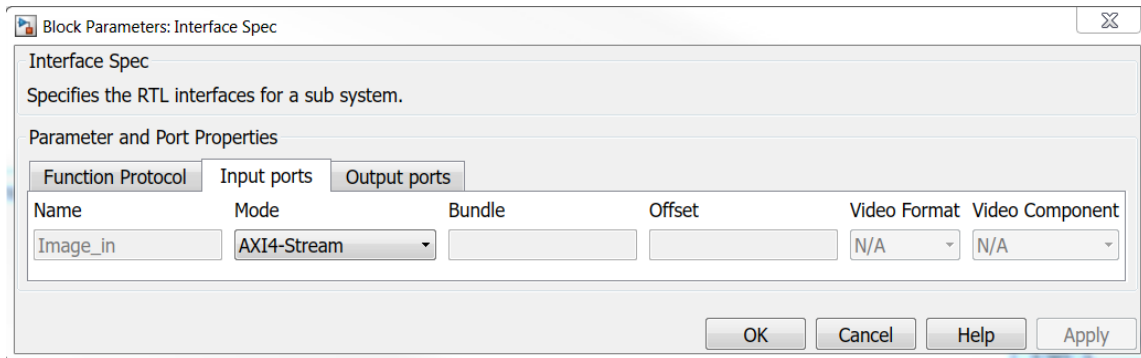
Choosing **System Generator** as the **Export type**, and clicking **Generate**, creates a synthesized RTL block that you can directly add to a System Generator design using the Vivado HLS block in System Generator.

In this lab, you create an IP using Model Composer and then use the synthesized RTL as a block in a System Generator design.

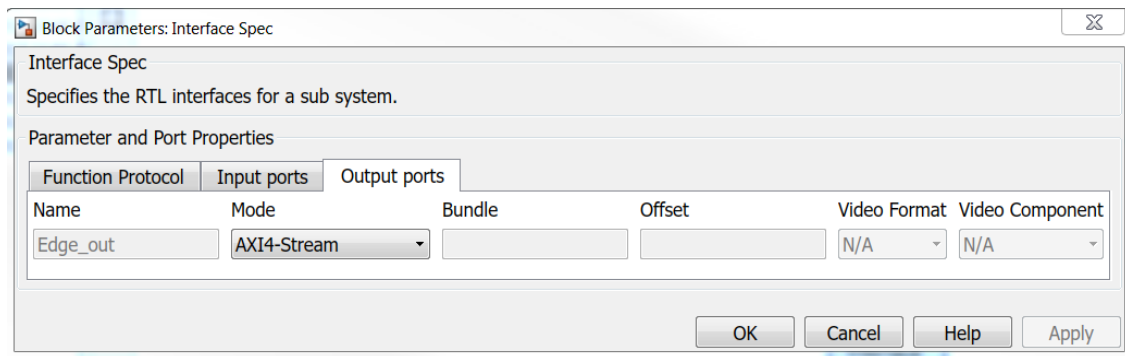
1. In the `ModelComposer_Tutorial/Lab3/ModelComposer_to_SysGen` folder, double-click `MoC_design.slx` to see the Model Composer design. The design is configured to have AXI4 streaming interfaces at both the input and output. This is done through the **Interface Spec** block within the **ModelComposerDesign** subsystem. Note that there are no structural changes required at the Simulink level to change interfaces for the IP.



**Figure 41: Interface Spec block**



**Figure 42: Interface Spec block Input Port Settings**



**Figure 43: Interface Spec block Output Port Settings**

2. Open the `followme_script.m` in MATLAB. This script will guide you through all the steps to import the Model Composer generated solution as block in System Generator.
3. Read the comments at the start of each section (labeled `Section 1` to `Section 8`) in the MATLAB script and execute each section one at a time (the start of each section is marked by a `%%` sign). You can click on **Run and Advance** to step through each section in the script. The sections are as follows:

a. `Section 1: Set up`

Open MATLAB for Model Composer and choose a video file as an input.

```
video_filename = 'vipmen.avi';

v = VideoReader(video_filename);
frame_height = v.Height;
frame_width = v.Width;
save video_handle v
```

b. `Section 2: Creating a System Generator solution from a Model Composer design.`

Model Composer allows you to export a design as a block into System Generator. The result of exporting a design from Model Composer to System Generator is a `solution` folder that you will import into the System Generator design using Vivado HLS block in System Generator.

```
open_system('MoC_design');
xmcGenerate('MoC_design');
```

c. Section 3: Serializing the input video

Serialize the input video which is required for use with the System Generator design which will do pixel-based processing.

```
stream_in = zeros(ceil(v.FrameRate*v.Duration*v.Height*v.Width),1);

i = 1;
while hasFrame(v)
    frame = rgb2gray(readFrame(v));
    a = reshape(frame',[],1);
    stream_in(i:i+length(a)-1) = a;
    i = i + length(a);
end

save stream_in stream_in
```

d. Section 4: Launch System Generator

Using System Generator currently requires launching a separate MATLAB session using the System Generator Launcher.

```
system('C:\Xilinx\Vivado\2018.x\bin\sysgen.bat')
```

**Note:** Where 'x' in 2018.x denotes the latest release.

e. Section 5: Import the generated solution into System Generator

Set up the Vivado HLS block in the System Generator design to point to the correct solution folder generated in Section 2.

```
open_system('sys_gen_AXI');
```

f. Section 6: Simulate the System Generator Design

Simulate the System Generator design and save the outputs into a MAT file. Note that the simulation will be slower than the Model Composer design since we are simulating the generated RTL and are doing an element-by-element based processing.

```
sim('sys_gen_AXI');
```

g. Section 7: De-serializing the output of the System Generator design.

This is a post-processing step that creates a frame-based video for playback using the outputs logged from the System Generator simulation.

```
load stream_out
load video_handle

disp(['Length of input stream is ',num2str(length(stream_in))])
disp(['Length of output stream is ',num2str(length(stream_out))])

outputVideo = VideoWriter('stream_out.avi');
outputVideo.FrameRate = v.FrameRate;
open(outputVideo)
```

The output is boolean. This is why we multiply the img by 255 so that imshow shows the image.

```

for i = 1:length(stream_out)/v.Height/v.Width
    img = reshape(stream_out((i-
    1)*v.Height*v.Width+1:i*v.Height*v.Width),v.Width,v.Height);
    writeVideo(outputVideo,255*img')
end
    
```

```
close(outputVideo);
```

h. Section 8: Play the de-serialized output using imshow.

```
imshow('stream_out.avi')
```

- The AXI4 stream uses three signals, DATA, READY, and VALID. The READY signal is a back pressure signal from the slave side to the master side indicating whether the slave side can accept new data.

As you examine the System Generator model in Section 5, pay attention to the labels on blocks for each signal to help you understand how the model is designed. For example, whenever the IP can no longer accept input, the READY signal (top right of the Vivado HLS block) puts pressure on the master side of the input AXI FIFO by resetting the READY signal. Likewise, the input AXI FIFO pressures the input stream by resetting its READY signal.

Note that in Simulink all the inputs to a block are to one side of the block, and all the outputs are on the opposite side. As such, all the slave or master signals are not bundled together on one side of the block as you might expect.

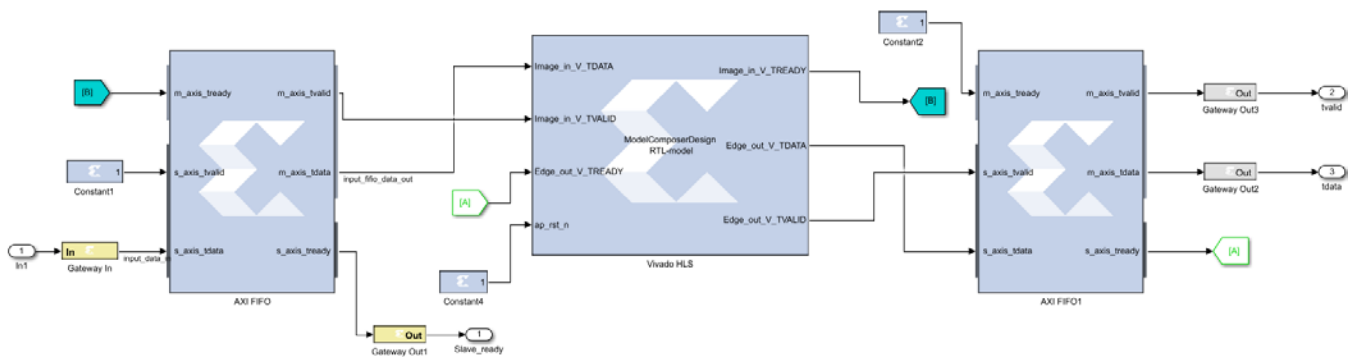


Figure 44: Corresponding System Generator Design

## Conclusion

In this lab, you learned:

- About the **Interface Spec** block terminology and parameter names.
- How to specify interfaces and to map them directly from the Simulink environment using the **Interface Spec** block.
- How Model Composer enables *push button IP creation* from your design in Simulink with the necessary interfaces.
- How the **Model Composer Hub** block in Model Composer helps move from algorithm to implementation.
- How to generate code files from the **Model Composer Hub** block and read them.
- How to set compilation targets to **C++ code**, **IP Catalog** and **System Generator**.

Some additional notes about Model Composer:

- Model Composer takes care of mapping interfaces as part of the code generation process and you don't have to take care of interleaving and de-interleaving color channels and interface connections at the design level.
- An **Interface Spec** block must be placed within the subsystem for which you intend to generate code.
- For the **C++ code** compilation target, Model Composer generates everything you would need to further optimize and synthesize the design using Vivado HLS.
- Model Composer automatically generates the test vectors and test benches for C/RTL cosimulation in Vivado HLS.
- Model Composer provides an option to export a design back into System Generator through the Vivado HLS block.
- When moving from a Model Composer design to System Generator, you move from an untimed C-based bit-true design to an RTL-based bit-true and cycle-accurate design.

The following `solution` directory contains the final Model Composer (\*.slx) files for this lab.

```
C:\ModelComposer_Tutorial\Lab3\solution
```

---

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