Addressing Thermal Challenges with Innovative Packaging Solutions

WP563 (v1.0) March 10, 2025 **White Paper**

Abstract

Deploying mid to high-end FPGAs and SoCs in demanding environments requires advanced thermal management solutions. This white paper presents AMD innovations in lidless packaging technology, which result in lower power consumption, reduced product cost and weight, and support for wider ambient temperature ranges. The flexibility for customers to choose the best thermal interface material (TIM) for their application further enhances thermal performance and end of life (EOL) reliability. AMD detailed thermal models and partnerships with thermal experts to ensure reliable solutions, positioning AMD at the forefront of high-performance, thermally efficient FPGA technology.

Introduction

As the electronics industry advances to smaller nodes, modern applications demand higher clock rates and performance. In 2014, Stanford Professor Mark Horowitz published a seminal paper describing the challenges that the semiconductor industry faces related to the breakdown of Dennard scaling and Moore's law. [Ref 1] While the jury might still be out on Moore's law, Dennard scaling has slowed, and higher performance comes at the expense of higher leakage. If we shrink die area and the power dissipated by the part does not decrease proportionally, thermal density will increase, which drives the need for more efficient thermal management solutions.

Product innovation requires new features and the ability to support higher compute density. Meanwhile, the market is driving the deployment of new products in more challenging environments, often with high ambient temperatures. Cooling these devices is a non-trivial exercise, particularly in extreme environments such as those found in common applications like wireless (55°C) and automotive (85°C) systems. Even more challenging are the extreme environments in space applications where the ambient temperature can fluctuate by more than 300°C. Here, active thermal control systems moderate the temperature to which the electronics are exposed, and heat is removed via fluid loops and external infrared radiators, increasing demands on thermal efficiency. In challenging environments, even modest improvements in thermal resistance can have significant benefits.

AMD has continued to innovate with Versal™ adaptive SoCs by hardening critical functions and interfaces, for example, multirate MAC (MRMAC), 600G channelized multirate Ethernet (DCMAC), AI Engines, and low-density parity check (LDPC). One key innovation in all Versal devices is the programmable network on chip (NoC), which provides high-bandwidth, deterministic connectivity infrastructure hardened on the chip. Collectively, these advances reduce the amount of programmable logic needed, paving the pathway to lower dynamic power, push button timing closure, and the possibility of using smaller, more efficient devices for a given task. For more details on the advantages of the Versal NoC, go to: *Optimize Design Efficiency with the Versal Adaptive SoC Programmable Network on Chip* (WP562).

The specific innovation presented in this white paper is AMD lidless packaging technology, a game changer that provides unparalleled system-level benefits. Lidless with stiffener ring packages should not be confused with bare-die lidless packaging. AMD lidless with stiffener ring packaging delivers a more efficient thermal solution and enables our customers to deploy products in almost any environment, both on, and off this planet!

Lidless Packaging with Stiffener Ring

In the Versal portfolio, AMD offers two packaging options: lidded, and lidless with a stiffener ring. While lidded packages provide additional mechanical protection to the die, lidless packages offer better thermal characteristics. See *Designing Heatsinks and Thermal Solutions for Xilinx Devices* (XAPP1377).

Bare-die packaging, commonly called "lidless packaging," is typically used for lower-density, cost-optimized products, such as the AMD Spartan™ UltraScale+™ family. In contrast, lidless packaging with a stiffener ring is employed for mid to high-end products such as Versal devices.

There is a direct relationship between die size and initial warpage, meaning that larger devices have higher warpage. Furthermore, the package and die experience warpage during the solder reflow process or when otherwise subjected to thermal fluctuations. The resulting die-to-heatsink coplanarity must be offset by the application of a thicker layer of TIM (TIM 1.5) between the die and heatsink. This added layer thickness worsens thermal performance.

In lidded packages, thermally induced warpage is less pronounced because of the added structural rigidity of the lid, but this comes at the cost of reduced thermal efficiency, due to the added thermal resistance of both the lid and the TIM (TIM 1) needed to mate the die to the lid. To achieve optimized performance for larger die, we need to remove the lid, while providing a solution to maintain rigidity.

Figure 1 provides insights into the differences between bare-die lidless and lidless with stiffener ring packaging. A unique feature of AMD lidless packages for mid-range and high-end devices is the addition of a stainless-steel stiffener ring around the periphery of the package substrate. The stiffener ring provides enhanced package rigidity (like the lid in lidded packages), which improves the overall package coplanarity. In addition to reducing warpage, the stiffener ring acts as a guide for the heatsink. This advancement benefits the thermal efficiency and reliability of lidless packaging for larger die.

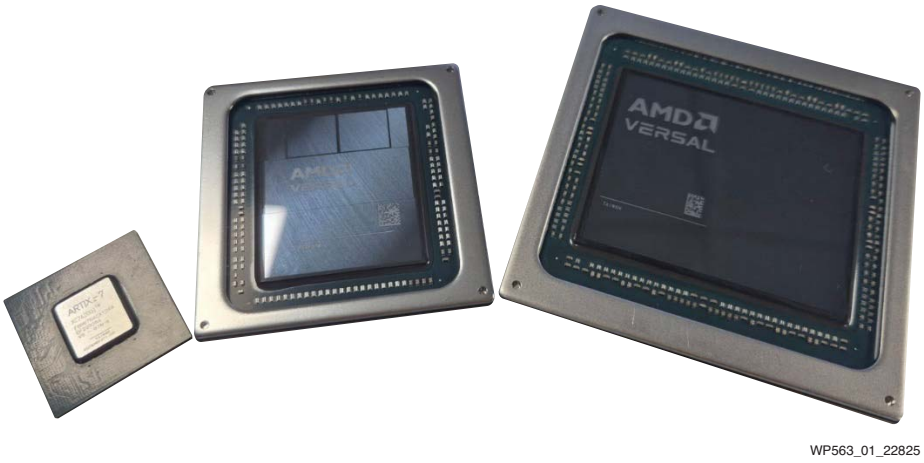

Figure 1: **Example of Bare-Die Lidless: Artix™ 7 FPGA, and Lidless with Stiffener Ring: Versal HBM and Versal Premium (VP1902) Adaptive SoCs**

Figure 2 illustrates a simplified cross-section of both lidless and lidded packages, highlighting the key thermal interface materials.

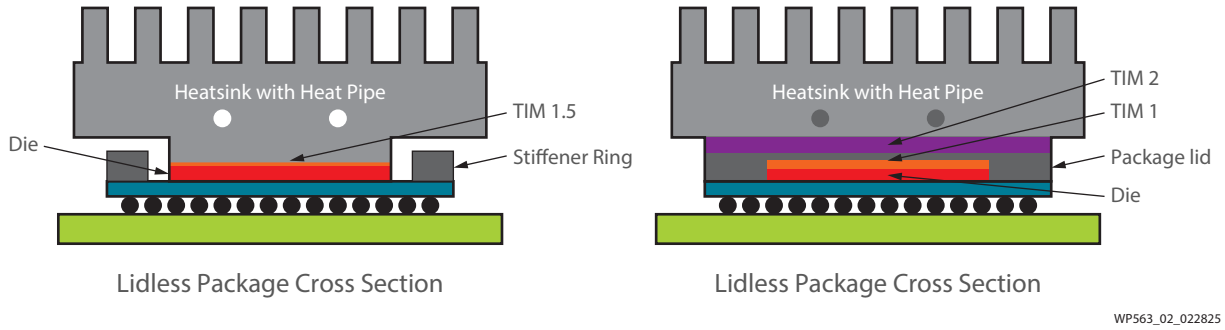

Figure 2: **Lidless Package (left) and Lidded Package (right)**

Comparing the lidded and lidless package cross-sections, we see that lidless packages enable mating of the die directly with the heatsink. In lidless packages, both the package lid and one TIM layer (TIM1) are removed.

Each added thermal interface material adds to the total thermal resistance. The thermal path is represented as follows:

For lidless packages:

$$\Theta_{jc} = \Theta_{silicon}$$

For lidded packages:

$$\Theta_{jc} = \Theta_{silicon} + \Theta_{TIM1} + \Theta_{lid}$$

Where:

$\Theta_{silicon} = [T_{J(max)} - T_{Case(avg)}] \div P_{total}$

$\Theta_{TIM1} = [T_{TIMBottom(avg)} - T_{TIMTop(avg)}] \div P_{total}$

$\Theta_{lid} = [T_{TIMTop(avg)} - T_{Case(avg)}] \div P_{total}$

By reducing the number of thermal boundary layers between the die and the heatsink, lidless packaging achieves a more efficient thermal solution and provides several key advantages:

- Reduced junction temperature - Lowers the junction temperature (Tj) compared to a lidded solution, improving thermal performance, and reducing leakage, which leads to lower overall power consumption.
- Higher reliability - While AMD advertises the same lifetime for lidless and lidded packages, it is also well understood that lowering operating junction temperatures results in increased system-level reliability, enabling a broader range of applications at a specific power density. Refer to *Device Reliability Report* (UG116) for device reliability data.
- Decreased junction-to-sink thermal resistance - This makes it possible to design a thermal solution that supports the same (or lower) Tj as a lidded package, with a smaller heatsink. This makes lidless packaging ideal for cost- and weight-sensitive applications.
- Increased thermal headroom - The design can support a wider ambient temperature (Ta) range versus lidded products, or the developer can push the clock rates higher to achieve better performance.

Lidless Packages with Stiffener Ring: Evaluation

AMD has invested in lidless packaging for FPGAs and adaptive SoCs for over a decade, aiming to deliver a robust and customer-ready solution. Traditionally, the industry has heavily leveraged thermal simulation as a part of packaging and IC design cycles. However, relying solely on simulation can fail to identify key variables early in the design process, resulting in a less optimal product. To address this, AMD decided to pursue a more practical approach.

Specifically, AMD developed a thermal test vehicle (TV) IC with 1,600 thermal sensors and heater cores. This innovative approach allowed AMD to model various device densities and applications, offering granular, localized heat generation. The TV IC enabled AMD to emulate various thermal scenarios across key applications and markets for AMD products. Figure 3, taken from an 2020 IEEE paper [Ref 2], shows a comparison of die thermal contours of a lidless package and a typical lidded package with the same die size (20 mm x 20 mm) and same power dissipation. The peak temperature in the lidless package is 70°C, which is 26°C lower than the peak temperature in the lidded package.

Figure 3: **Lidded and Lidless with Stiffener with Heat Map**

Before taping out our Zynq™ UltraScale+ RFSoC product family, AMD built both TV-lidded and lidless prototypes and mapped an example 5G application to the TV. The test parameters were specified as 50W power dissipation (Pd), an ambient temperature (Ta) of 45°C, and passive cooling with minimal airflow.

This evaluation allowed AMD to compare the future RFSoC device in lidded and lidless packaging, using identical boundary conditions and thermal solutions. In evaluating this example on the TV, AMD measured a 24°C reduction in junction temperature for the lidless with stiffener packaging. See Figure 4.

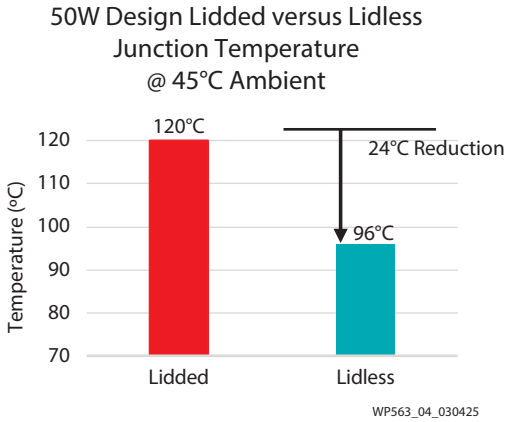

Figure 4: **5G Application Mapped to Lidded and Lidless with Stiffener TVs**

But how does this translate into real-world benefits for a packaged part? To answer this question, we can evaluate the thermal performance of the Versal VM1802, available in both lidded and lidless packages. As seen in Figure 5, the thermal resistance (θjc) for the VM1802 in lidless packaging with a stiffener ring provides an eleven times reduction compared to the VM1802 in lidded packaging, demonstrating the significant improvement in thermal capabilities offered by the AMD lidless design.

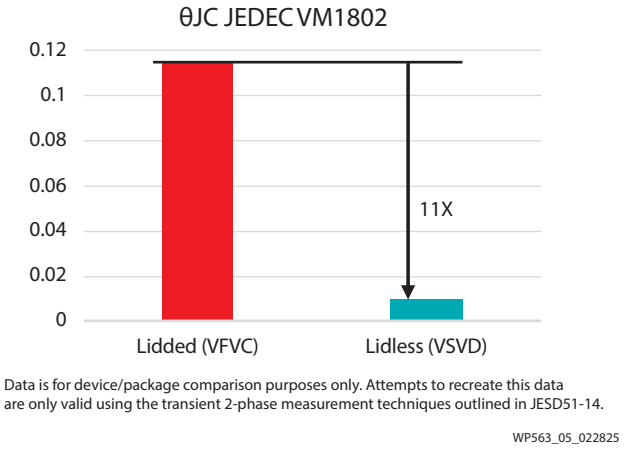

Figure 5: **JESD51-14 Data for VM1802 Device**

It is also important to consider that reducing θjc leads to a corresponding reduction in junction temperature, which reduces leakage. As shown in Figure 6, for every 10°C reduction in junction temperature, static power decreases by approximately 25%, and for every 20°C reduction, static power is reduced by about 50%. This results in lower total power consumption, improved power efficiency at the same level of performance, and provides more thermal margin, which allows for higher performance or reduced thermal solution costs.

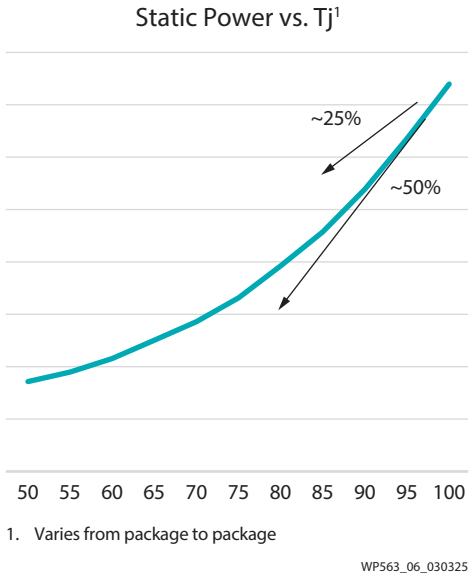

Figure 6: **Static Power Savings from Reduced Junction Temperature**

The precise value of this reduction depends on factors such as product family, core voltage, and junction temperature. The AMD Power Design Manager should be used to estimate this. Here, the developer

specifies two parameters - the maximum ambient temperature for the design, and the effective θja of the thermal solution.

AMD lidless with stiffener ring packaging offers superior thermal efficiency, resulting in lower junction temperatures. This translates to significant static power savings compared to competing devices.

Extending the Thermal Envelope

While AMD has been innovating at the FPGA packaging level, TIM suppliers have made important advancements that further enhance thermal transfer. Specifically, we refer to phase change material (PCM) TIMs. The combination of AMD and industry innovations not only boosts beginning of life (BOL) thermal performance but also ensures superior End of Life (EOL) thermal performance.

BOL is the first phase of the product life cycle. At BOL, the product has minimal wear and tear and has closer to "ideal" performance. EOL is the final phase, where the product has undergone significant usage and can experience performance degradation. Figure 7 illustrates this concept.

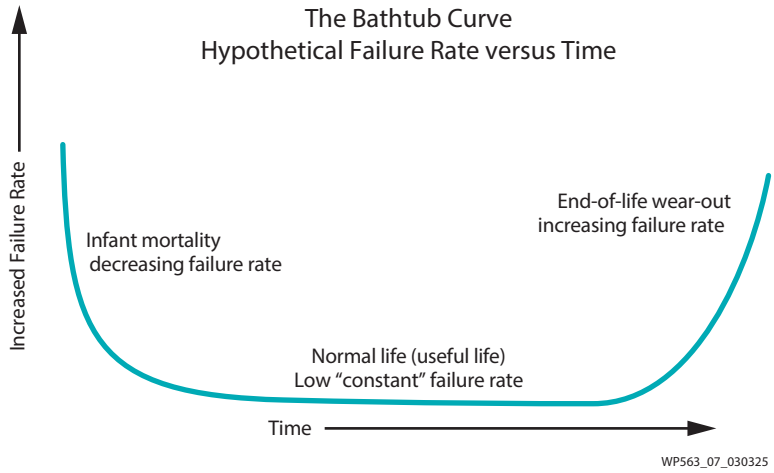

Figure 7: **Failure Rate Frequency Versus Time**

Good thermal performance at BOL and EOL is crucial to ensure product reliability, efficiency, and longevity. Improving thermal performance across the entire lifecycle prevents overheating and helps to reduce premature failure.

A key innovation recommended by AMD is the use of an etch pattern on the base of the heatsink to enhance thermal performance. To maximize the benefit of this pattern, a PCM TIM is necessary. As the temperature of the PCM TIM rises, it transitions from solid to liquid, increasing the surface area at the interface. Additionally, the combination of PCM and etch pattern helps reduce the impact of warpage. The combination of this etch pattern and PCM TIMs improves both BOL and EOL thermal performance.

Figure 8 illustrates the etch pattern on the base of the heatsink - a textured surface with multiple grooves, as opposed to a conventional flat base design. Experiments show that this design acts as a reservoir for the PCM, which, unlike more rigid TIM materials, can flow to fill any gaps caused by warpage. The etch pattern increases the overall TIM contact surface area by approximately 10%. Another widespread problem alleviated by this design relates to gas bubbles in the TIM, commonly trapped during the application of

the TIM, which reduce thermal transfer. With the application of the etch pattern, gas bubbles are pushed into and trapped in the grooves or driven out of the interface between the device and TIM altogether. This ensures that the (un-grooved) flat areas have direct TIM contact with the die, and thus, better thermal conductivity. Furthermore, as shown in Figure 9, larger TIM particles flow into the etched grooves, which reduces bond line thickness (BLT). This etched pattern aims to decrease overall thermal resistance, increase the effective thermal conductivity of the TIM, and improve heat flow from the die to the heat sink.

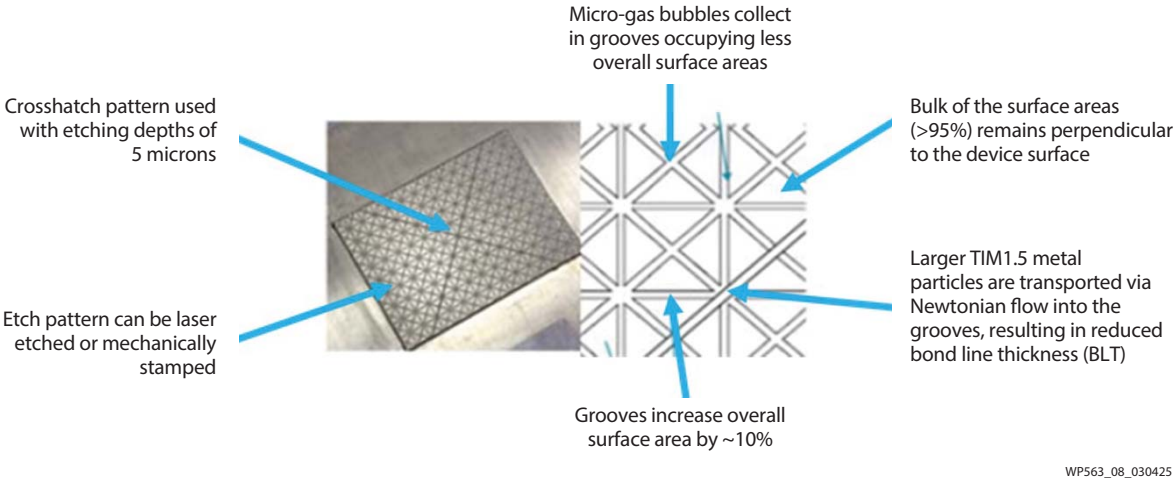

Figure 8: **Thermal Performance Improvement through Etch Pattern**

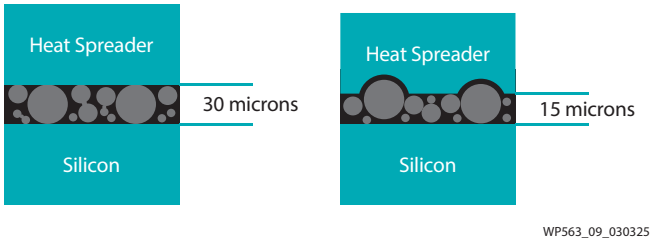

Figure 9: **Larger Particles Flow into Etched Grooves**

One added advantage of lidless packaging is the flexibility to choose the thermal interface material for a specific design. With lidless packages, all TIMs are applied after the device is soldered to the board. In contrast, lidded packages require TIM1 (die to lid) to be applied by the vendor, and the selected material must withstand reflow temperatures exceeding 220°C. PCM TIMs cannot be employed in lidded packages due to the maximum temperature limitations (e.g., 150°C) of currently available products. With lidless packages, TIM 1.5 is not subject to high reflow temperatures, meaning the developer can select the best TIM for their specific application.

With lidded packages, the designer must rely on the integrity of the in-package TIM. If vendor quality is lacking, voids can be present in the die-to-lid TIM layer and negatively impact product thermal performance and longevity. Lidless packaging offers the end customer full control to evaluate TIM integrity without removing a lid (lidded package lid removal voids warranty) or to employ non-destructive analysis techniques such as CSAM. With lidless packages, it is simple to remove the heatsink and evaluate the integrity of the TIM. Figure 10 illustrates TIM integrity of AMD lidless with stiffener ring packaging and PCM TIMs over one-thousand thermal cycles.

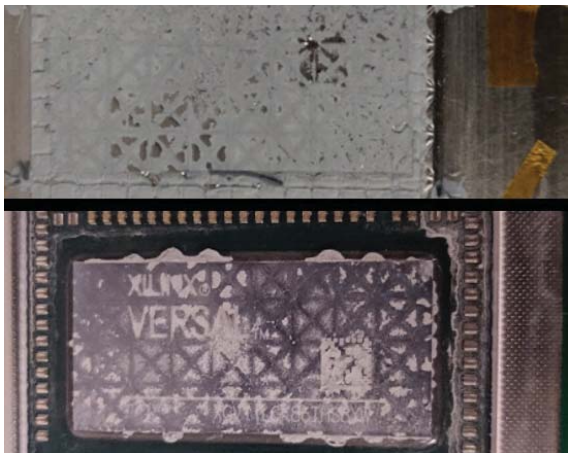

Figure 10: **AMD Versal Device Lidless TIM Coverage After One Thousand Thermal Cycles**

The choice of TIM affects thermal performance over the lifecycle and EOL performance of the product. AMD conducts lifetime testing to ensure BOL and EOL performance. Additionally, AMD has partnered with Nokia, Laird, and Shin-Etsu to investigate the long-term performance impact of TIM selection. Readers can refer to an IEEE paper [Ref 3] for additional details of this research.

Again, we emphasize that with lidless packages, customers can choose any TIM 1.5 based on design requirements. The investigations conducted by AMD are for reference purposes.

Thermal Models Availability and Partners

Thermal validation is crucial when deploying mid to high-end FPGAs, especially in high ambient environments or high-density designs. To support this, AMD provides thermal models, compatible with industry-leading simulation tools like Siemens Flotherm and Ansys Icepak for all FPGA and SoC products. These models are available to registered customers via the AMD download site. There are three types of models available for AMD devices:

1. **JEDEC Model**: Available for UltraScale+ and earlier AMD product families, these models offer a good balance of simulation speed and accuracy, however, as thermal density and ambient temperature increase more accurate thermal modeling is required.
2. **Simplified Detailed Model**: Supported for Versal devices. This model provides detailed information about the package while removing specific features to speed up simulation time. For example, in a lidless package with a stiffener ring, the model does not include the stiffener ring, reducing meshing requirements. This model is ideal for early evaluation and thermal design iterations.
3. **Full Detailed Model**: Supported for Versal devices. This model includes comprehensive details of the package, such as micro traces inside the substrate, interposer, and silicon die, along with the stiffener ring. With increased accuracy, the detailed model should be used for design sign-off.

The BGA array is modeled as a solid block with effective conductivity in both simplified and full detailed models.

The AMD strategy for thermal modeling is straightforward. Across all AMD product families, the FPGA die and transceivers are monolithic. Furthermore, the stacked silicon interconnect (SSI) technology used by AMD to integrate multiple FPGA die into a single package, allows for uniform power modeling, resulting in a simplified methodology for thermal analysis and more consistent thermal performance. Power analysis of some competing products requires that the user have specific power mappings for each die within the package (i.e., transceiver tiles). While the power mapping technique can be acceptable for designs that have a fixed architecture, any changes made to the design, such as to transceiver rates or location, can drastically impact thermal performance, require additional modeling cycles, and potentially require changes to the production thermal management solution.

To further support customers, AMD has partnered with thermal experts through the AMD Alliance program, enabling customers to collaborate directly with these partners for thermal evaluation, simulation, design, or heatsink supply.

Conclusion

Thermal validation is essential for deploying mid to high-end FPGAs, particularly in demanding environments. AMD lidless with stiffener ring packaging offers several key benefits:

- Enhanced Thermal Performance: By reducing the number of thermal interfaces between the die and heatsink, lidless packaging decreases thermal resistance. This results in lower junction temperatures, which improves thermal performance and reduces leakage power. Consequently, this leads to lower total power consumption and greater power efficiency.
- Cost and Weight Reduction: The simplified thermal design of lidless packaging reduces cost and weight while supporting the same junction temperature as lidded packages, without compromising performance.
- Wider Ambient Temperature Range: The improved thermal performance of AMD lidless packaging supports a broader ambient temperature range compared to competing products. This is particularly beneficial for applications in high ambient environments, such as automotive, space, and wireless.
- Flexibility in TIM Selection: Lidless packaging provides flexibility in selecting thermal interface materials (TIM). Since TIMs are applied after the device is soldered to the board, more efficient TIMs can be used at the critical die-to-heatsink interface. This enhances thermal performance and ensures better EOL performance.
- System-level performance and mean time between failures: Cooler devices support higher clock rates and more densely packed designs. Furthermore, any decrease in junction temperature offers a corresponding reduction in device (and system) failure rates.
- Comprehensive Thermal Models: AMD offers detailed thermal models for all its products, designed for industry-leading simulation tools like Siemens Flotherm and Ansys Icepak. These models aid customers in designing refined thermal management solutions and are available for download by registered customers on the AMD website.
- Partnerships with Thermal Experts: To further support customers, AMD has partnered with thermal experts through the AMD Alliance program. This enables customers to collaborate directly with these partners for thermal evaluation, simulation, design, or heatsink supply, ensuring robust and reliable thermal solutions.

Overall, AMD innovations in packaging and thermal management ensure that AMD FPGA and adaptive SoC products deliver superior performance, reliability, and efficiency, even in extreme applications and markets. These advancements position AMD as a leader in providing high-performance, thermally efficient solutions for varied applications. Are you curious to better understand the benefits of AMD lidless with stiffener packages? Use AMD thermal models to simulate one of our lidless packages. If you are trying to decide between lidded and lidless packages, you can back-annotate the simulated, estimated θ_{JA} value into the AMD Power Design Manager and you will be able to see the difference for yourself.

When comparing AMD to competitors, make sure that you are accounting for the significant advantages afforded by AMD lidless packages with stiffener ring.

Finally, if you are interested in learning more, head over to the AMD Power Efficiency webpage, where you can find additional information about topics such as Thermal Design and Power Estimation, including a link to download the latest version of the AMD Power Design Manager tool.

References

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Revision History

The following table shows the revision history for this document.

Section	Revision Summary
3/10/2025 Version 1.0	
Initial AMD release.	

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