

Introduction

The Xilinx Multi-Channel On-chip Peripheral Bus Double Data Rate Synchronous DRAM (MCH OPB DDR2 SDRAM) controller for Xilinx FPGAs provides a DDR2 SDRAM controller that connects to the OPB and multiple channel interfaces and provides the control interface for DDR2 SDRAMs. It is assumed that the reader is familiar with DDR2 SDRAM and the MCH protocol.

Features

The Xilinx MCH OPB DDR2 SDRAM Controller is a soft IP core designed for Xilinx FPGAs and contains the following features:

- Parameterizable number of channel (MCH) interfaces that can be configured with the Xilinx Cachelink (XCL) protocol (see "Reference Documents" on page 53)
- Optional OPB interface & indeterminate burst support
- Performs device initialization sequence upon power-up and reset conditions for ~200 us
- Performs auto-refresh cycles
- Supports DDR2 SDRAM self refresh mode
- Supports CAS latencies of 3, 4 and 5
- Supports target word first XCL cacheline transactions of 1, 4, 8 and 16 words
- Supports 16-bits, 32-bits and 64-bits DDR2 SDRAM devices
- Provides big-endian connections to memory devices
- Supports multiple (up to 4) external DDR2 memory banks
- Selectable On Die Termination (ODT)
- Supports DDR2 burst size of 4
- Supports differential DQS
- Capable to separate DDR2 clock frequency domain from MCH/OPB clock frequency domain. Following combinations of frequencies are tested:
 - MCH/OPB clock: 66 MHz & DDR2 clock: 133 MHz
 - MCH/OPB clock: 100 MHz & DDR2 clock: 133 MHz
 - MCH/OPB clock: 100 MHz & DDR2 clock: 200 MHz

LogiCORE™ Facts		
Core Specifics		
Supported Device Family	QPro™-R Virtex™-II, QPro Virtex-II, Virtex-II, Virtex-II Pro, Virtex-4, Spartan™-3	
Version of Core	mch_opb_ddr2	v1.00a
Resources Used		
	Min	Max
Slices	Please refer to Table 13 on page 48 , Table 14 on page 50 and Table 15 on page 52	
LUTs		
FFs		
Block RAMs		
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs	None	
Design Tool Requirements		
Xilinx Implementation Tools	ISE 8.1i or later	
Verification	N/A	
Simulation	ModelSim SE/EE 6.0a or later	
Synthesis	XST 8.1i or later	
Support		
Support provided by Xilinx, Inc.		

MCH OPB DDR2 SDRAM Controller Design Parameters

To allow the user to create a MCH OPB DDR2 SDRAM controller that is uniquely tailored for the system, certain features are parameterizable in the MCH OPB DDR2 SDRAM controller design. This allows the user to have a design that only utilizes the resources required by the system and runs at the best possible performance. The features that are parameterizable in the MCH OPB DDR2 SDRAM controller are shown in [Table 1](#).

Table 1: MCH OPB DDR2 SDRAM Controller Design Parameters

Generic	Feature / Description	Parameter Name	Allowable Values	Default Value	VHDL Type
MCH OPB DDR2 SDRAM Controller Features					
G1	Target FPGA family	C_FAMILY	virtex2p, spartan3, virtex4	virtex2p	string
G2	Include support for registered DIMM	C_REG_DIMM	0 = DDR2 device is not registered DIMM 1 = DDR2 device is registered DIMM	0	integer
G3	Include logic to create extra setup time on DDR2 address and control signals ^[1]	C_EXTRA_TSU	0 = Don't include logic to support extra setup time 1 = Include logic to support extra setup time	0	integer
G4	Supported number of external DDR2 SDRAM memory banks ^[2]	C_NUM_BANKS_MEM	1 - 4	1	integer
G5	Number of generated clock pairs supplied to the DDR2 memory	C_NUM_CLK_PAIRS	1 - 4	1	integer
G6	Include logic to support asynchronous DDR2 SDRAM clock from OPB bus clock	C_DDR_ASYNC_SUPPORT	1 = Include logic to separate DDR2 SDRAM clock domain from MCH/OPB clock domain 0 = Not supported	1	integer
G7	Enable differential DQS capability for DDR2 memory devices	C_DDR_ENABLE_DIFF_DQS	0 = Disable differential DQS logic 1 = Enable differential DQS logic	0	integer
G8	Specify number of IDELAYCTRL modules to instantiate for Virtex-4 implementation	C_NUM_IDELAYCTRL	1 - 20	1	integer
G9	On Die Termination selection	C_DDR2_ODT_SETTING	0, 75, 150 0 = ODT will be disabled 75 = ODT enabled and On Die Terminating resistance (Rtt) will be 75 Ω 150 = ODT enabled and Rtt will be 150 Ω	0	integer

Table 1: MCH OPB DDR2 SDRAM Controller Design Parameters (Continued)

Generic	Feature / Description	Parameter Name	Allowable Values	Default Value	VHDL Type
G10	Include OPB Slave Interface	C_INCLUDE_OPB_IPIF	0 = Don't include OPB IPIF 1 = Include OPB IPIF	1	integer
G11	Include logic to support OPB bursts	C_INCLUDE_OPB_BURST_SUPPORT	0 = Don't include logic to support OPB bursts 1 = Include logic to support OPB bursts	0	integer
G12	Arbitration mode between OPB and MCH interfaces	C_PRIORITY_MODE	0 = Fixed priority mode	0	integer
G13	Data bus width for MCH and OPB (if included in design)	C_MCH_OPB_DWIDTH	32	32	integer
G14	Address bus width for MCH and OPB (if included in design)	C_MCH_OPB_AWIDTH	32	32	integer
G15	MCH/OPB clock period (ps)	C_MCH_OPB_CLK_PERIOD_PS	10000, 15000	10000	integer
MCH Interface					
G16	Number of MCH channels	C_NUM_CHANNELS	0 - 4	2	integer
G17	MCH protocol ^{[3][4]}	C_MCHx_PROTOCOL	0 = XCL protocol (see "Reference Documents" on page 53)	0	integer
G18	Depth of MCH access buffer ^{[3][5]}	C_MCHx_ACCESSBUF_DEPTH	4, 8, 16	16	integer
G19	Depth of MCH read data buffer ^{[3][6]}	C_MCHx_RDDATABUF_DEPTH	0, 4, 8, 16	16	integer
G20	Cacheline size ^[3] (in number of 32-bit words)	C_XCLx_LINESIZE	1, 4, 8, 16	4	integer
G21	Write transfer type ^{[3][7]}	C_XCLx_WRITEXFER	0 = No write transfers 1 = Single transfers only 2 = Cacheline transfers only	1	integer
G22	Include timeout counter	C_INCLUDE_TIMEOUT_CNTR	0 = Don't include an acknowledge timeout counter	0	integer

Table 1: MCH OPB DDR2 SDRAM Controller Design Parameters (Continued)

Generic	Feature / Description	Parameter Name	Allowable Values	Default Value	VHDL Type
G23	Number of clocks to wait for transfer acknowledge from the DDR2 controller before issuing a timeout error	C_TIMEOUT	1 - 512	16	integer
DDR2 SDRAM Controller Features					
G24	Load Mode Register command cycle time (ps)	C_DDR_TMRD	Note ^[8]	15000	integer
G25	Write Recovery Time (ps)	C_DDR_TWR	Note ^[8]	15000	integer
G26	Write-to-Read Command Delay (Tck)	C_DDR_TWTR	Note ^[8]	1	integer
G27	Delay after ACTIVE command before PRECHARGE command (ps)	C_DDR_TRAS	Note ^[8]	45000	integer
G28	Delay after ACTIVE command before another ACTIVE or AUTOREFRESH command (ps)	C_DDR_TRC	Note ^[8]	65000	integer
G29	Delay after AUTOREFRESH before another command (ps)	C_DDR_TRFC	Note ^[8]	75000	integer
G30	Delay after ACTIVE command before READ/WRITE command (ps)	C_DDR_TRCD	Note ^[8]	21000	integer
G31	Delay after ACTIVE command for a row before an ACTIVE command for another row (ps)	C_DDR_TRRD	Note ^[8]	10000	integer
G32	Delay after a PRECHARGE command (ps)	C_DDR_TRP	Note ^[8]	20000	integer
G33	Average periodic refresh command interval (ps)	C_DDR_TREFI	Note ^[8]	7800000	integer
G34	Self refresh exit delay before issuing an ACTIVE command	C_DDR_TXSR	Note ^[8]	80000	integer

Table 1: MCH OPB DDR2 SDRAM Controller Design Parameters (Continued)

Generic	Feature / Description	Parameter Name	Allowable Values	Default Value	VHDL Type
G35	ACTIVE command for a row before an ACTIVE command for another row when crossing internal 4 banks (ps)	C_DDR_TFAW	Note ^{[8][9]}	50000	integer
G36	CAS Latency	C_DDR_CAS_LAT	3, 4, 5	3	integer
G37	Cumulative data width of DDR2 SDRAM	C_DDR_DWIDTH	16, 32, 64	16	integer
G38	DDR2 SDRAM address width	C_DDR_AWIDTH	See note ^[10]	13	integer
G39	DDR2 SDRAM column address width	C_DDR_COL_AWIDTH	See note ^[10]	9	integer
G40	DDR2 SDRAM bank address width	C_DDR_BANK_AWIDTH	2, 3 ^[10]	2	integer
G41	DDR2 SDRAM clock period (ps)	C_DDR_CLK_PERIOD_PS	5000, 7500	5000	integer
Address Space					
G42	Base Address for Memory Bank x (x = 0 to 3)	C_MEMx_BASEADDR	Valid address ^{[11][12]}	-	std_logic_vector
G43	High Address for Memory Bank x (x = 0 to 3)	C_MEMx_HIGHADDR	Valid address ^{[11][12]}	-	std_logic_vector

Table 1: MCH OPB DDR2 SDRAM Controller Design Parameters (Continued)

Generic	Feature / Description	Parameter Name	Allowable Values	Default Value	VHDL Type
Simulation Only					
G44	DDR2 Initialization time for simulation ^[13] (ps)	C_SIM_INIT_TIME_PS	≥ 200 us	2000000 00	integer

Notes:

- C_EXTRA_TSU parameter is only valid when C_REG_DIMM = 0. When C_EXTRA_TSU = 1, the design creates extra setup time on the following signals: DDR_CS_n, DDR_RAS_n, DDR_CAS_n, DDR_WEN, DDR_BankAddr and DDR_Addr. Setting C_EXTRA_TSU = 1 is useful for certain memory board applications with high input capacitance on DDR2 control and address connections.
- C_NUM_BANKS_MEM specifies the number of DDR2 SDRAM memory banks with identical device characteristics. All the DDR2 SDRAM device characteristics specified in parameters, G33 through G50, are applicable for all memory banks. The C_NUM_BANKS_MEM parameter specifies the size of the DDR_CS_n signal(s).
- This design can accommodate up to 4 channels. The generics associated with the MCH interfaces are designated with a C_MCH_x prefix where x indicates the channel number and must be value between 0 and 3.
- C_MCH_x_PROTOCOL = 0 (or XCL, Xilinx Cachelink) is the only supported protocol.
- The depth of the MCH access buffer (C_MCH_x_ACCESSBUF_DEPTH) must be large enough to hold a cacheline write. C_MCH_x_ACCESSBUF_DEPTH ≥ C_XCL_x_LINESIZE for optimal performance.
- If the master connected to the MCH interface can consume data as soon as it is available (i.e., instruction cache masters) the Read Data buffer depth can be set to zero to save resources and eliminate extra latency. Otherwise, the Read Data buffer depth must be sized to accommodate any latency the master may have in reading data from this buffer.
- If the master connecting to the channel x will only perform read transfers (i.e., instruction cache masters) set C_XCL_x_WRITEXFER = 0 to save resources.
- Values are as per DDR2 JEDEC standard.
- C_DDR_TFAW setting is only valid when C_DDR_BANK_AWIDTH = 3.
- C_DDR_AWIDTH + C_DDR_COL_AWIDTH + C_DDR_BANK_AWIDTH + log₂(C_DDR_DWIDTH/8) must be < C_MCH_OPB_AWIDTH - 1.
- This design can accommodate up to 4 banks of DDR2 memory. The address range generics are designated as C_MEM0_BASEADDR, C_MEM1_BASEADDR, C_MEM0_HIGHADDR, C_MEM1_HIGHADDR, etc.
- The range specified by C_MEM_x_BASEADDR and C_MEM_x_HIGHADDR must comprise a complete, contiguous power of two range such that range = 2^m, and the m least significant bits of C_MEM_x_BASEADDR must be zero. Any MCH or OPB transaction can be mapped to any DDR2 memory bank.
- This parameter adjusts the initialization time of the DDR2 for simulation only. Must be ≥ 200 us.

Allowable Parameter Combinations

The user must be aware of the following parameter combinations:

- The MCH OPB DDR2 SDRAM controller supports up to 4 banks of memory. Each bank of memory has its own independent base address and address range. Each address range specified by C_MEMx_BASEADDR and C_MEMx_HIGHADDR must comprise a complete, contiguous power of two range such that range = 2^m , and the m least significant bits of C_MEMx_BASEADDR must be zero.
- The range specified by these parameters should not exceed the MCH OPB DDR2 SDRAM memory space.
- The OPB slave interface is only included in this design if C_INCLUDE_OPB_IPIF = 1. When C_INCLUDE_OPB_IPIF = 0, the C_INCLUDE_OPB_BURST_SUPPORT is unused.
- The parameter C_EXTRA_TSU is ignored when C_REG_DIMM = 1.

Optimal MCH Parameter Settings

If an XCL channel is connected to a master that will only perform read transactions, then C_XCLx_WRITEXFER should be set to 0 indicating that no write transfers will be performed. This will reduce the channel logic to only contain logic for read transactions.

If an XCL channel is connected to a master that can consume data as soon as its available, then C_MCHx_RDDATABUF_DEPTH for that channel should be set to 0. This will eliminate the read data buffer and eliminate the latency that would normally exist in reading data from this buffer. If the master can not consume data as soon as its available, then C_MCHx_RDDATABUF_DEPTH for that channel should be set to accommodate any latency the master has in reading data from the Read Data buffer.

Optimal performance will be achieved when the buffer depth of the Access buffer is set greater than or equal to the line size of the channel ($C_MCHx_ACCESSBUF_DEPTH \geq C_XCLx_LINESIZE$).

MCH OPB DDR2 SDRAM Controller I/O Signals

Table 2 provides a summary of all MCH OPB DDR2 SDRAM controller input/output (I/O) signals.

Table 2: MCH OPB DDR2 SDRAM Controller Pin Descriptions

Port	Signal Name	Interface	I/O	Initial State	Description
DDR2 SDRAM Signals					
P1	DDR_Clk [0:C_NUM_CLK_PAIRS-1]	DDR2	O	0	DDR2 SDRAM clock
P2	DDR_Clk _{in} [0:C_NUM_CLK_PAIRS-1]	DDR2	O	1	DDR2 SDRAM inverted clock
P3	DDR_CKE [0:C_NUM_BANKS_MEM-1]	DDR2	O	0	DDR2 SDRAM clock enable(s)
P4	DDR_CS _n [0:C_NUM_BANKS_MEM-1]	DDR2	O	1	Active low DDR2 SDRAM chip select(s)
P5	DDR_RAS _n	DDR2	O	1	Active low DDR2 SDRAM row address strobe
P6	DDR_CAS _n	DDR2	O	1	Active low DDR2 SDRAM column address strobe
P7	DDR_WEn	DDR2	O	1	Active low DDR2 SDRAM write enable
P8	DDR_DM[0:C_DDR_DWIDTH/8-1]	DDR2	O	0	DDR2 SDRAM data mask
P9	DDR_BankAddr[0:C_DDR_BANK_AWIDTH-1]	DDR2	O	0	DDR2 SDRAM bank address
P10	DDR_Addr[0:C_DDR_AWIDTH-1]	DDR2	O	0	DDR2 SDRAM address
P11	DDR_DQ _o [0:C_DDR_DWIDTH-1]	DDR2	O	0	Output data to DDR2 SDRAM
P12	DDR_DQ _i [0:C_DDR_DWIDTH-1]	DDR2	I	-	Input data from DDR2 SDRAM
P13	DDR_DQ _t [0:C_DDR_DWIDTH-1]	DDR2	O	0	3-state control for DDR2 SDRAM data buffers
P14	DDR_DQS _o [0:C_DDR_DWIDTH/8-1]	DDR2	O	0	Output data strobe to DDR2 SDRAM
P15	DDR_DQS _i [0:C_DDR_DWIDTH/8-1]	DDR2	I	-	Input data strobe from DDR2 SDRAM
P16	DDR_DQS _t [0:C_DDR_DWIDTH/8-1]	DDR2	O	1	3-state control for DDR2 SDRAM data strobe buffers
P17	DDR_DQS _n _o [0:C_DDR_DWIDTH/8-1]	DDR2	O	0	Output differential data strobe to DDR2 SDRAM
P18	DDR_DQS _n _i [0:C_DDR_DWIDTH/8-1]	DDR2	I	-	Input differential data strobe from DDR2 SDRAM
P19	DDR_DQS _n _t [0:C_DDR_DWIDTH/8-1]	DDR2	O	1	3-state enable for DDR2 SDRAM differential data strobe buffers
P20	DDR_ODT[0:C_NUM_BANKS_MEM-1] ^[1]	DDR2	O	0	On Die Termination (ODT) signal for DDR2 SDRAM
P21	DDR_Init_done	DDR2	O	0	Indicates that the DDR2 initialization is complete
Clock Signals					

Table 2: MCH OPB DDR2 SDRAM Controller Pin Descriptions (Continued)

Port	Signal Name	Interface	I/O	Initial State	Description
P22	Device_Clk ^[2]	CLK	I	-	Device clock
P23	Device_Clk_n ^{[2][3]}	CLK	I	-	Device clock phase shifted by 180 degrees
P24	Device_Clk90_in ^[2]	CLK	I	-	Device clock phase shifted by 90 degrees
P25	Device_Clk90_in_n ^{[2][3]}	CLK	I	-	Device clock phase shifted by 270 degrees
P26	DDR_Clk90_in ^{[2][3]}	CLK	I	-	DDR2 SDRAM feedback clock shifted by 90 degrees
P27	DDR_Clk90_in_n ^{[2][3]}	CLK	I	-	DDR2 SDRAM feedback clock shifted by 270 degrees
P28	Clk_200 ^{[2][4]}	CLK	I	-	200 MHz clock input used in Virtex-4 implementation for IDELAYCTRL module
P29	Cal_Clk ^{[2][4]}	CLK	I	-	1/4 Clk_200 clock input used in Virtex-4 implementation
OPB Slave Signals ^{[5][6]}					
P30	OPB_Select	OPB	I	-	OPB select
P31	OPB_RNW	OPB	I	-	OPB read not write
P32	OPB_ABus[0:C_MCH_OPB_AWIDTH-1]	OPB	I	-	OPB address bus
P33	OPB_DBus[0:C_MCH_OPB_DWIDTH-1]	OPB	I	-	OPB data bus
P34	OPB_BE[0:C_MCH_OPB_DWIDTH/8-1]	OPB	I	-	OPB byte enables
P35	OPB_seqAddr	OPB	I	-	OPB sequential address
P36	Sl_xferAck	OPB	O	0	OPB DDR2 SDRAM controller transfer acknowledge
P37	Sl_errAck	OPB	O	0	OPB DDR2 SDRAM controller error acknowledge
P38	Sl_toutSup	OPB	O	0	OPB DDR2 SDRAM controller time-out suppress
P39	Sl_retry	OPB	O	0	OPB DDR2 SDRAM controller retry
P40	Sl_DBus[0:C_MCH_OPB_DWIDTH-1]	OPB	O	0	OPB DDR2 SDRAM controller OPB slave data bus
MCH Signals ^[7]					
P41	MCH_OPB_Clk	MCH	I	-	MCH/OPB clock
P42	MCH_OPB_Rst	MCH	I	-	MCH/OPB reset
P43	MCHx_Access_Control (x = 0 to 3)	MCH	I	-	Control signal to the Access buffer of MCH interface x (x = 0 to 3). This signal indicates the type of access to be performed (read or write) and the size of the access (byte, halfword, or word)

Table 2: MCH OPB DDR2 SDRAM Controller Pin Descriptions (Continued)

Port	Signal Name	Interface	I/O	Initial State	Description
P44	MCHx_Access_Data(0:C_MCH_OPB_DWIDTH-1) (x = 0 to 3)	MCH	I	-	Write Data to the Access buffer of MCH interface x (x = 0 to 3)
P45	MCHx_Access_Write (x = 0 to 3)	MCH	I	-	Write signal to the Access buffer of MCH interface x (x = 0 to 3)
P46	MCHx_Access_Full (x = 0 to 3)	MCH	O	0	Indicator that the Access buffer of MCH interface x is full (x = 0 to 3)
P47	MCHx_ReadData_Control (x = 0 to 3)	MCH	O	1	Control signal for the Read Data buffer of MCH interface x (x = 0 to 3). This signal indicates if the data from the Read Data buffer is valid
P48	MCHx_ReadData_Data(0:C_MCH_OPB_DWIDTH-1) (x = 0 to 3)	MCH	O	0	Read data from the Read Data buffer of MCH interface x (x = 0 to 3)
P49	MCHx_ReadData_Read (x = 0 to 3)	MCH	I	-	Read signal to the Read Data buffer of MCH interface x (x = 0 to 3)
P50	MCHx_ReadData_Exists (x = 0 to 3)	MCH	O	0	Indicator that the Read Data buffer of MCH interface x is non-empty (x = 0 to 3)
P51	DDR_Sleep	System	I	-	Rising edge on this signal enters the DDR2 SDRAM self refresh mode. A minimum period of 50us after the assertion of DDR_Sleep is required before MCH_OPB_Rst can be asserted
P52	DDR_WakeUp	System	I	-	This signal indicates whether the DDR2 SDRAM must go through the power-up initialization after reset, or if only the sequence to exit the self refresh mode needs to be executed. This signal is sampled when reset negates and therefore should be asserted before MCH_OPB_Rst negates

Notes:

1. When this signal is asserted high, the selected Rtt value is specified by the parameter C_DDR2_ODT_SETTING. For more information please refer to section **On Die Termination (ODT)**.
2. For more information on clocking options please refer to section **"DDR2 Clocking" on page 31**.
3. Input signal is unused when targeting for Virtex-4 architecture. It is recommended to ground these inputs.
4. Input signal is unused when targeting architecture other than Virtex-4. It is recommended to ground these inputs.
5. Please refer to the IBM OPB Architecture Specification for more detailed information on these signals.
6. OPB signals are not available when C_INCLUDE_OPB_IPIF = 0.
7. MCH signals are unavailable when C_NUM_CHANNELS = 0, with the exception of MCH_OPB_Clk and MCH_OPB_Rst.

Parameter-Port Dependencies

The dependencies between the MCH OPB DDR2 SDRAM controller design parameters and I/O signals are shown in **Table 3**. **Table 3** shows when certain features are parameterized out of the design, the related logic will no longer be part of the design. The unused input signals and related output signals are set to a specified value.

Table 3: Parameter-Port Dependencies

Generic or Port	Parameter	Affects	Depends	Description
Design Parameters				
G1	C_FAMILY	P23, P25, P26, P27, P28, P29	-	P23, P25, P26, P27 are not used when C_FAMILY = virtex4. P28, P29 are not used when C_FAMILY ≠ virtex4.
G4	C_NUM_BANKS_MEM	P3, P4, P20	-	Specifies the number of DDR2 SDRAM memory banks.
G5	C_NUM_CLK_PAIRS	P1, P2	-	Number of generated DDR2 clock pairs
G7	C_DDR_ENABLE_DIFF_DQS	P17, P18, P19	-	Input signals are unused and output signals are set to the default value when C_DDR_ENABLE_DIFF_DQS = 0.
G10	C_INCLUDE_OPB_IPIF	P30, P31, P32, P33, P34, P35, P36, P37, P38, P39, P40	-	Input signals are unused and output signals are set to the default value when C_INCLUDE_OPB_IPIF = 0.
G11	C_INCLUDE_OPB_BURST_SUPPORT	-	G9	Unused if C_INCLUDE_OPB_IPIF = 0.
G13	C_MCH_OPB_DWIDTH	P33, P34, P40, P44, P48	-	Affects OPB data width when C_INCLUDE_OPB_IPIF = 1.
G14	C_MCH_OPB_AWIDTH	P32	-	Affects OPB address width when C_INCLUDE_OPB_IPIF = 1.
G16	C_NUM_CHANNELS	P43, P44, P45, P46, P47, P48, P49, P50	-	Input signals are unused and output signals are set to the default value when C_NUM_CHANNELS = 0.
G46	C_DDR_DWIDTH	P8, P11 - P19	-	Specified DDR2 memory data width.
G47	C_DDR_AWIDTH	P10	-	
G49	C_DDR_BANK_AWIDTH	P9	-	
G3	C_EXTRA_TSU	-	G2	Valid only when C_REG_DIMM = 0.
I/O Signals				
P1	DDR_Clk [0:C_NUM_CLK_PAIRS-1]	-	G5	The number of clock pairs is generated based on C_NUM_CLK_PAIRS.
P2	DDR_Clk _n [0:C_NUM_CLK_PAIRS-1]	-	G5	The number of inverted clock pairs is generated based on C_NUM_CLK_PAIRS.
P3	DDR_CKE [0:C_NUM_BANKS_MEM-1]	-	G4	The number of clock enables is generated based on C_NUM_BANKS_MEM.

Table 3: Parameter-Port Dependencies (Continued)

Generic or Port	Parameter	Affects	Depends	Description
P4	DDR_CS _n [0:C_NUM_BANKS_MEM-1]	-	G4	The number of chip selects is generated based on C_NUM_BANKS_MEM.
P8	DDR_DM[0:C_DDR_DWIDTH/8-1]	-	G37	Width of data mask signal depends on generic C_DDR_DWIDTH.
P9	DDR_BankAddr[0:C_DDR_BANK_AWIDTH]	-	G40	Bank address width depends on generic C_DDR_BANK_AWIDTH.
P10	DDR_Addr[0:C_DDR_AWIDTH]	-	G38	DDR2 address width depends on generic C_DDR_AWIDTH.
P11	DDR_DQ_o[0:C_DDR_DWIDTH-1]	-	G37	Data output width depends on generic C_DDR_DWIDTH.
P12	DDR_DQ_i[0:C_DDR_DWIDTH-1]	-	G37	Data input width depends on generic C_DDR_DWIDTH.
P13	DDR_DQ_t[0:C_DDR_DWIDTH-1]	-	G37	Data 3-state enable signal width depends on generic C_DDR_DWIDTH.
P14	DDR_DQS_o[0:C_DDR_DWIDTH/8-1]	-	G37	Output data strobe width depends on generic C_DDR_DWIDTH.
P15	DDR_DQS_i[0:C_DDR_DWIDTH/8-1]	-	G37	Input data strobe width depends on generic C_DDR_DWIDTH.
P16	DDR_DQS_t[0:C_DDR_DWIDTH/8-1]	-	G37	3-state enable data strobe width depends on generic C_DDR_DWIDTH.
P17	DDR_DQSn_o[0:C_DDR_DWIDTH/8-1]	-	G37	Output differential data strobe width depends on generic C_DDR_DWIDTH. Output is driven high when C_DDR_ENABLE_DIFF_DQS = 0.
P18	DDR_DQSn_i[0:C_DDR_DWIDTH/8-1]	-	G37	Input differential data strobe width depends on generic C_DDR_DWIDTH. Input signals is unused when C_DDR_ENABLE_DIFF_DQS = 0.
P19	DDR_DQSn_t[0:C_DDR_DWIDTH/8-1]	-	G37	3-state enable differential data strobe width depends on generic C_DDR_DWIDTH. Signals is unused when C_DDR_ENABLE_DIFF_DQS = 0.
P20	DDR_ODT[0:C_NUM_BANKS_MEM-1]	-	G4	On Die Termination (ODT) signal width depends on generic C_NUM_BANKS_MEM.
P23	Device_Clk_n	-	G1	Unused when C_FAMILY = virtex4.
P25	Device_Clk90_in_n	-	G1	Unused when C_FAMILY = virtex4.
P26	DDR_Clk90_in	-	G1	Unused when C_FAMILY = virtex4.
P27	DDR_Clk90_in_n	-	G1	Unused when C_FAMILY = virtex4.
P28	Clk_200	-	G1	Unused when C_FAMILY ≠ virtex4.
P29	Cal_Clk	-	G1	Unused when C_FAMILY ≠ virtex4.
P30	OPB_Select	-	G10	Unused when C_INCLUDE_OPB_IPIF = 0.

Table 3: Parameter-Port Dependencies (Continued)

Generic or Port	Parameter	Affects	Depends	Description
P31	OPB_RNW	-	G10	Unused when C_INCLUDE_OPB_IPIF = 0.
P32	OPB_ABus[0:C_MCH_OPB_AWIDTH-1]	-	G10, G14	Unused when C_INCLUDE_OPB_IPIF = 0.
P33	OPB_DBus[0:C_MCH_OPB_DWIDTH-1]	-	G10, G13	Unused when C_INCLUDE_OPB_IPIF = 0.
P34	OPB_BE[0:C_MCH_OPB_DWIDTH/8-1]	-	G10, G13	Unused when C_INCLUDE_OPB_IPIF = 0.
P35	OPB_seqAddr	-	G10	Unused when C_INCLUDE_OPB_IPIF = 0.
P36	SI_xferAck	-	G10	Unused when C_INCLUDE_OPB_IPIF = 0.
P37	SI_errAck	-	G10	Unused when C_INCLUDE_OPB_IPIF = 0.
P38	SI_toutSup	-	G10	Unused when C_INCLUDE_OPB_IPIF = 0.
P39	SI_retry	-	G10	Unused when C_INCLUDE_OPB_IPIF = 0.
P40	SI_DBus[0:C_MCH_OPB_DWIDTH-1]	-	G10, G13	Unused when C_INCLUDE_OPB_IPIF = 0.
P43	MCHx_Access_Control (x = 0 to 3)	-	G16	Unused when C_NUM_CHANNELS = 0.
P44	MCHx_Access_Data[0:C_MCH_OPB_DWIDTH-1] (x = 0 to 3)	-	G13, G16	Unused when C_NUM_CHANNELS = 0.
P45	MCHx_Access_Write (x = 0 to 3)	-	G16	Unused when C_NUM_CHANNELS = 0.
P46	MCHx_Access_Full (x = 0 to 3)	-	G16	Unused when C_NUM_CHANNELS = 0.
P47	MCHx_ReadData_Control (x = 0 to 3)	-	G16	Unused when C_NUM_CHANNELS = 0.
P48	MCHx_ReadData_Data[0:C_MCH_OPB_DWIDTH-1] (x = 0 to 3)	-	G13, G16	Unused when C_NUM_CHANNELS = 0.
P49	MCHx_ReadData_Read (x = 0 to 3)	-	G16	Unused when C_NUM_CHANNELS = 0.
P50	MCHx_ReadData_Exists (x = 0 to 3)	-	G16	Unused when C_NUM_CHANNELS = 0.

Connecting to Memory

Big-Endian Memory Data Types and Organization

DDR2 SDRAM memory can be accessed as byte (8 bits), halfword (2 bytes), word (4 bytes) or double word (8 bytes) depending on the size of the bus to which the processor is attached. From the point of view of the MCH/OPB, data is organized as big-endian. The bit and byte labeling for the big-endian data types is shown below in [Figure 1](#).

Byte address	n	n+1	n+2	n+3	n+4	n+5	n+6	n+7	Double Word								
Byte label	0	1	2	3	4	5	6	7									
Byte significance	MSB							LSB									
Bit label	0									63							
Bit significance	MSBit									LSBit							
Byte address	n		n+1		n+2		n+3		Word								
Byte label	0		1		2		3										
Byte significance	MSB						LSB										
Bit label	0									31							
Bit significance	MSBit									LSBit							
Byte address	n	n+1							Halfword								
Byte label	0	1															
Byte significance	MSB	LSB															
Bit label	0															15	
Bit significance	MSBit															LSBit	
Byte address	n								Byte								
Byte label	0																
Byte significance	MSB																
Bit label	0							7									
Bit significance	MSBit							LSBit									

Figure 1: Big-Endian Data Types

Memory to MCH OPB DDR2 SDRAM Controller Connections

The data and address signals at the MCH OPB DDR2 SDRAM controller are labeled with big-endian bit labeling (for example, D(0:31), D(0) is the MSB), whereas most memory devices are either endian agnostic (they can be connected either way) or little-endian D(31:0) with D(31) as the MSB.

Caution must be exercised with the connections to the external memory devices to avoid incorrect data and address connections.

[Table 6](#) shows the correct mapping of MCH OPB DDR2 SDRAM controller pins to DDR2 SDRAM device pins.

Table 6: MCH OPB DDR2 SDRAM controller interconnect to DDR2 SDRAM

Description	MCH OPB DDR2 SDRAM Controller Signals (MSB:LSB)	DDR2 SDRAM Signals (MSB:LSB)
Data Bus	DDR_DQ[0:C_DDR_DWIDTH - 1]	DQ[C_DDR_DWIDTH - 1:0]
Bank Address	DDR_BankAddr[0:C_DDR_BANK_AWIDTH - 1]	BA[C_DDR_BANK_AWIDTH - 1:0]
Address	DDR_Addr[0:C_DDR_AWIDTH - 1]	A[C_DDR_AWIDTH - 1:0]
Data Strobe	DDR_DQS[0:C_DDR_DWIDTH/8 - 1]	UDQS, LDQS
Differential Data Strobe	DDR_DQSn[0:C_DDR_DWIDTH/8 - 1]	UDQS#, LDQS#
Data Mask	DDR_DM[0:C_DDR_DWIDTH/8 - 1]	UDM, LDM

Example 1: 32-bit Connection

Figure 2 illustrates an example of connecting memory to the MCH OPB DDR2 SDRAM controller design. The example shown here has the following specified parameters:

- C_NUM_BANKS_MEM = 1
- C_DDR_DWIDTH = 32
- C_DDR_BANK_AWIDTH = 2
- C_DDR_AWIDTH = 13
- C_DDR_ENABLE_DIFF_DQS = 0

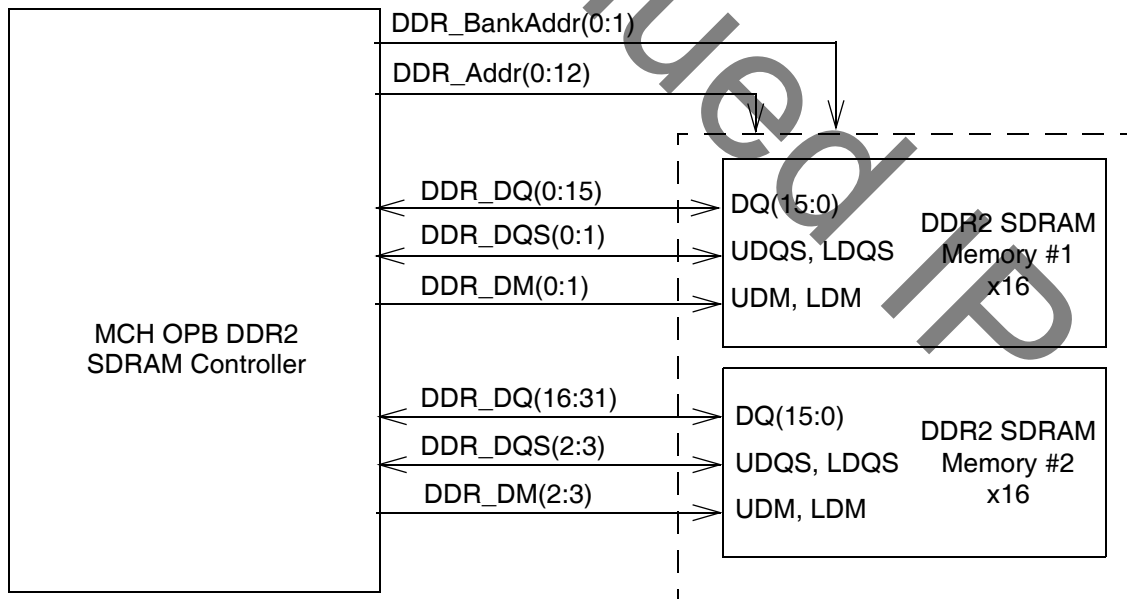


Figure 2: MCH OPB DDR2 SDRAM Controller Connection Example to 32-bit DDR2 SDRAM

Example 2: 16-bit Connection

Figure 3 illustrates an example of connecting memory to the MCH OPB DDR2 SDRAM controller for 16-bit DDR2 SDRAM. The example shown here has the following specified parameters:

- C_NUM_BANKS_MEM = 1
- C_DDR_DWIDTH = 16
- C_DDR_BANK_AWIDTH = 2
- C_DDR_AWIDTH = 13
- C_DDR_ENABLE_DIFF_DQS = 1

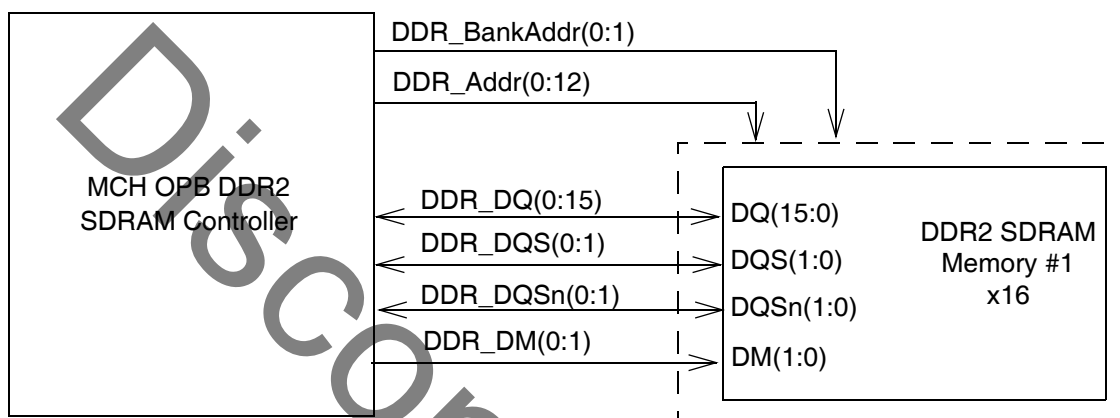


Figure 3: MCH OPB DDR2 SDRAM Controller Connection Example to 16-bit DDR2 SDRAM

DDR2 SDRAM Address Mapping

An address offset is calculated based on the width of the DDR2 SDRAM data bus. The DDR2 SDRAM column address is then mapped to the MCH OPB address bus, followed by the row address and bank address.

An address offset is calculated based on the width of the DDR2 SDRAM data bus. The DDR2 SDRAM column address is then mapped to the MCH OPB address bus, followed by the row address and bank address.

The MCH OPB address bus bit locations for the DDR2 SDRAM column, row and bank addresses are calculated as shown in Table 7 and Table 8.

Table 7: DDR2 SDRAM Address Offset Calculations

Variable	Equation
ADDR_OFFSET	$\log_2(C_DDR_DWIDTH/8)$
COLADDR_STARTBIT	$C_MCH_OPB_AWIDTH - (C_DDR_COL_AWIDTH + ADDR_OFFSET)$
COLADDR_ENDBIT	$COLADDR_STARTBIT + C_DDR_COL_AWIDTH - 1$
ROWADDR_STARTBIT	$COLADDR_STARTBIT - C_DDR_AWIDTH$
ROWADDR_ENDBIT	$ROWADDR_STARTBIT + C_DDR_AWIDTH - 1$
BANKADDR_STARTBIT	$ROWADDR_STARTBIT - C_DDR_BANK_AWIDTH$
BANKADDR_ENDBIT	$BANKADDR_STARTBIT + C_DDR_BANK_AWIDTH - 1$

Table 8: DDR2 SDRAM - Address Bus Assignments

DDR2 SDRAM Address	MCH OPB Address Bus
Column Address	MCH_OPB_ABus(COLADDR_STARTBIT to COLADDR_ENDBIT)
Row Address	MCH_OPB_ABus(ROWADDR_STARTBIT to ROWADDR_ENDBIT)
Bank Address	MCH_OPB_ABus(BANKADDR_STARTBIT to BANKADDR_ENDBIT)

Table 9 and Table 10 show an example of the mapping between the MCH or OPB address and the DDR2 SDRAM address when the data width of the DDR2 SDRAM is 16 and the data width of the MCH/OPB bus is 32, the column address width is 9, the row address width is 13 and the bank address width is 2.

Table 9: MCH OPB Example DDR2 SDRAM Address Offset Calculations

Variable	Equation	Value
ADDR_OFFSET	$\log_2(C_DDR_DWIDTH/8)$	$\log_2(16 / 8) = 1$
COLADDR_STARTBIT	$C_MCH_OPB_AWIDTH - (C_DDR_COL_AWIDTH + ADDR_OFFSET)$	$32 - (9 + 1) = 22$
COLADDR_ENDBIT	$COLADDR_STARTBIT + C_DDR_COL_AWIDTH - 1$	$22 + (9 - 1) = 30$
ROWADDR_STARTBIT	$COLADDR_STARTBIT - C_DDR_AWIDTH$	$22 - 13 = 9$
ROWADDR_ENDBIT	$ROWADDR_STARTBIT + C_DDR_AWIDTH - 1$	$9 + 13 - 1 = 21$
BANKADDR_STARTBIT	$ROWADDR_STARTBIT - C_DDR_BANK_AWIDTH$	$9 - 2 = 7$
BANKADDR_ENDBIT	$BANKADDR_STARTBIT + C_DDR_BANK_AWIDTH - 1$	$7 + 2 - 1 = 8$

Table 10: MCH OPB DDR2 SDRAM Controller Address Bus Assignment Example

DDR2 SDRAM Address	MCH or OPB Address Bus
Column Address	MCH_OPB_ABus(22:30) & '0'
Row Address	MCH_OPB_ABus(9:21)
Bank Address	MCH_OPB_ABus(7:8)

IMPORTANT: Virtex-4, Virtex-II Pro and Spartan-3 IO pairs share input and output clock signals. Since the DDR registers in the IO blocks use both of the input and output clock signals, the ports assigned to the IO pairs must use the same input and output clocks. Care should be taken when making port IO assignments. The DDR_DQ and DDR_DM signals use the system clock as the output clock and the DDR_DQS signals use a 90 degree phase shift of the system clock as the output clock. Therefore, a DDR_DQS signal should not be assigned with a DDR_DQ signal or a DDR_DM signal in an IO pair.

Note this MCH OPB DDR2 SDRAM controller design utilizes the DDR registers in the FPGA IO blocks, and must be targeted to FPGA families that support this feature.

The DDR_DQ and DDR_DQS buses are 3-stateable, the user should pullup these signals in the FPGA IO blocks or external to the FPGA in the board design. Note that the MCH OPB DDR2 SDRAM controller design will drive the DQS signals to a high value '1' during the IDLE state so only one MCH OPB DDR2 SDRAM controller can be used to control a DDR2 SDRAM, i.e., two MCH OPB DDR2 SDRAM controllers can not share the same DDR2 SDRAM.

MCH OPB DDR2 SDRAM Controller Design

The block diagram for the MCH OPB DDR2 SDRAM controller is shown in [Figure 4](#). The MCH OPB DDR2 SDRAM controller consists of the MCH OPB IPIF and the DDR2 SDRAM controller. The MCH OPB IPIF provides the bus protocol and Multi-Channel (MCH) interface. The DDR2 SDRAM controller provides the DDR2 SDRAM interface, including the control state machines, initialization logic and I/O registers.

The separation of the Command State Machine and the Data State Machine allows for the application of commands to the DDR2 while data reception/transmission is in progress. Overlapping the DDR2 SDRAM commands with the data transfer when accessing data in the same row of the same bank allows for more optimal DDR2 SDRAM operation.

The MCH OPB DDR2 SDRAM controller consists of:

- a. The MCH OPB IPIF module provides the interface between the MCH and OPB connections to the DDR2 SDRAM controller.
- b. The Init State Machine module is responsible for initialization sequence of commands that are issued to the DDR2 SDRAM upon power up or self refresh.
- c. The Command State Machine is responsible to issue commands (read/write, self refresh/auto refresh, precharge etc.) to the DDR2 SDRAM after the completion of initialization.
- d. The Data State Machine is responsible for controlling the flow of data to and from the DDR2 SDRAM.
- e. The Write Async FIFO module separates the DDR2 SDRAM clock domain from the MCH/OPB clock domain. This allows the MCH OPB DDR2 SDRAM controller to operate on two independent frequencies.
- f. The Tap Control & Data Tap Increment modules calibrate the IDELAY tap value required to center align the data with respect to internal read clock for Virtex-4 devices.
- g. The Reg Unreg module is responsible to register the commands issued to the DDR2 SDRAM when the parameter C_REG_DIMM = 1.
- h. The IO Reg module is responsible to register the control and data signals, to and from the DDR2 SDRAM.
- i. The Read Data Path module is responsible for storing the data captured from IO Reg module in to an asynchronous FIFO and will transfer the same to the MCH/OPB.
- j. The Counters module incorporates logic to count various DDR2 SDRAM timing parameters and enable Command State Machine to issue commands at the end of the count.
- k. The Multiple Data Width module is instantiated when the data width of the DDR memory is equal to or greater than the data width of the OPB or MCH channels. In this controller, the Multiple Data Width module will be instantiated when the C_DDR_DWIDTH = 32 or C_DDR_DWIDTH = 64.
- l. FIFO Read Control module is responsible to generate read enable signal to the Async FIFO used in the Write Async FIFO module.
- m. Module Clock Generator is responsible to generate the complemented clocks (DDR_Clk & DDR_Clkn) to the DDR2 SDRAM.
- n. The IDELAYCTRL module(s) are specific to Virtex-4 devices. The IDELAYCTRL module requires a 200 MHz clock and controls the tap value of the IDELAY modules instantiated in the IO Reg module.

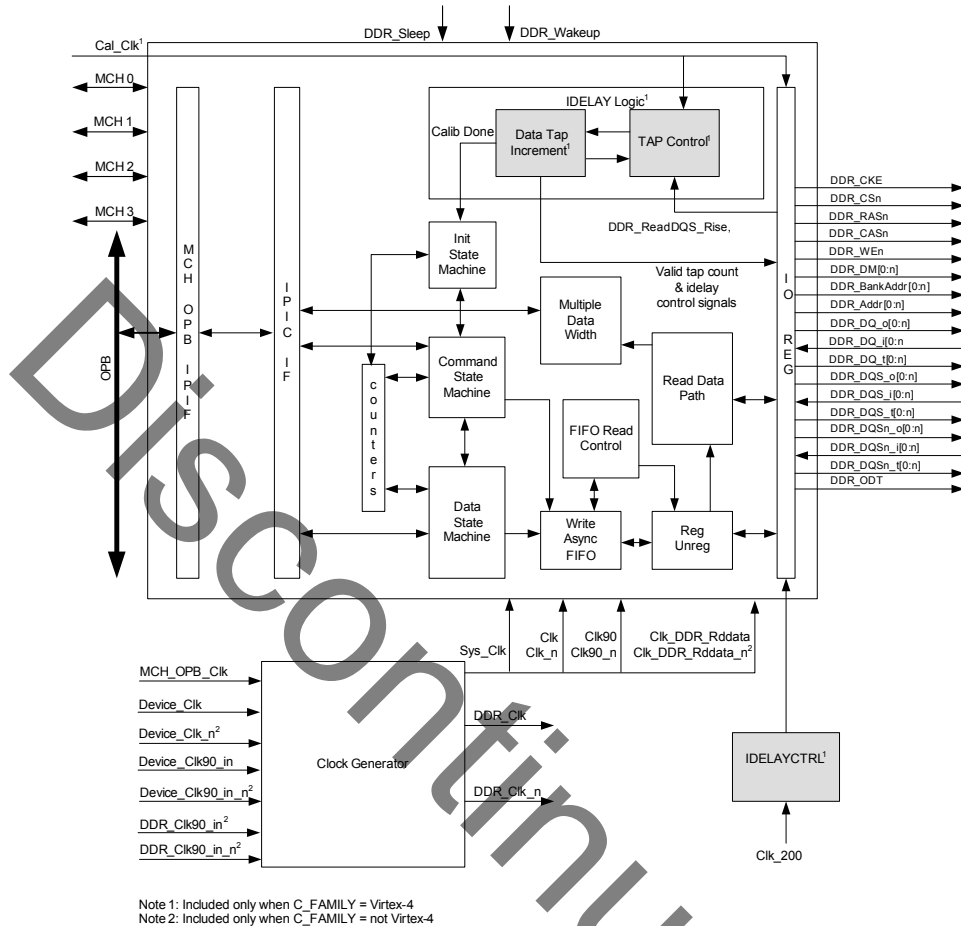


Figure 4: MCH OPB DDR2 SDRAM Controller Block Diagram

Self Refresh

The MCH OPB DDR2 controller is capable of placing the DDR2 SDRAM into self refresh mode. When the DDR2 SDRAM is placed in to self refresh mode, the contents of memory are saved due to the memory itself issuing refresh cycles.

DDR_Sleep and DDR_Wakeup are two inputs to the MCH OPB DDR2 SDRAM controller to support the DDR2 SDRAM self refresh mode. These are discrete input signals and must be generated at the system level, they are not derived from the interface.

A rising edge of the DDR_Sleep signal will cause the MCH OPB DDR2 SDRAM controller to execute the command sequences required to place the DDR2 SDRAM into self refresh. MCH_OPB_Rst is then asserted to place the entire system into reset. A minimum period of 50 us from the assertion of DDR_Sleep to the assertion of MCH_OPB_Rst is required to insure the DDR2 SDRAM is in the self refresh mode. Note that the MCH OPB DDR2 SDRAM controller does not provide the timing for the reset assertion, this should be done at the system level. Please refer to Figure 5 for information on the timing relationships of these signals.

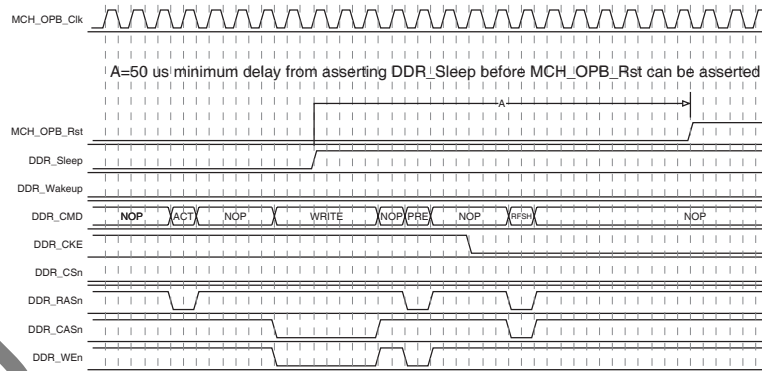


Figure 5: Entering DDR2 Self Refresh

The DDR_WakeUp signal is used to inform the MCH OPB DDR2 SDRAM controller if the power-up initialization sequence needs to be performed or if the sequence to instruct the DDR2 SDRAM to exit self refresh needs to be performed. If the DDR_WakeUp signal is de-asserted when MCH_OPB_Rst de-asserted, the MCH OPB DDR2 SDRAM controller will perform the initialization sequence for DDR2 SDRAM. If the DDR_WakeUp signal is asserted when MCH_OPB_Rst negates, the MCH OPB DDR2 SDRAM controller will instruct the DDR2 SDRAM to exit the self refresh mode. Note that the DDR_WakeUp signal must be at its desired level at least 5 clock periods before MCH_OPB_Rst negates. It is assumed that the clock is stable before MCH_OPB_Rst de-asserted. Please refer to Figure 6 for information on the timing relationships of these signals.

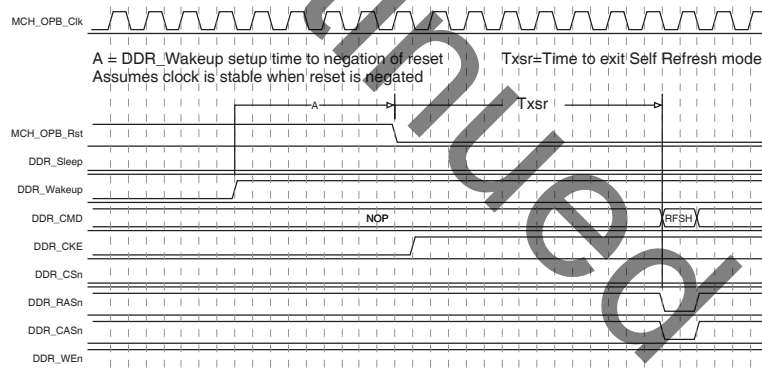


Figure 6: Exiting DDR2 Self Refresh

Init State Machine

DDR2 SDRAM must be powered-up and initialized in a predefined manner. After power supplies and all the clocks are stable, the DDR2 SDRAM requires a 200 us delay prior to applying an executable command.

The Init State Machine provides the 200 us delay and the sequencing of the required DDR2 SDRAM start-up commands. It instructs the command state machine to send the proper commands in the proper sequence to the DDR2 SDRAM. This state machine starts execution after reset and returns to the IDLE state when reset is applied.

When the initialization sequence has been completed, the DDR_Init_done signal is asserted.

Note that after reset has been applied, the 200 us delay is again implemented before any commands are issued to the DDR2 SDRAM. The 200 us delay must be accounted for simulation as well as the delay of the command sequence.

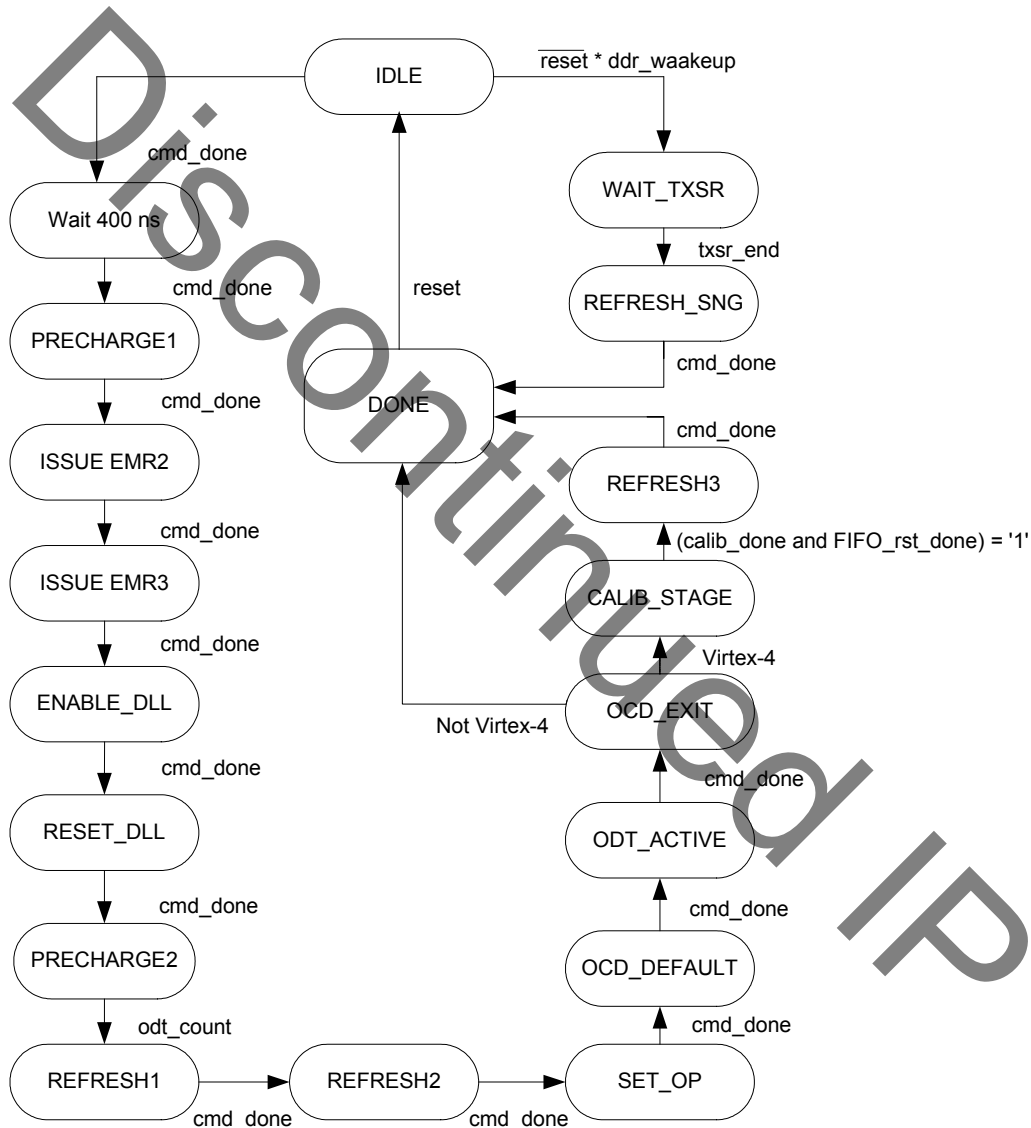


Figure 7: Init State Machine

Command State Machine

The Command State Machine provides the address bus and commands signals to the DDR2 SDRAM. It sends the enable signal to the Data State Machine to start the reception/transmission of data. If a burst transaction is in progress or a second-

any transaction has been received, the Command State Machine will send the next command to the DDR2 SDRAM while data reception/transmission is still in progress to optimize the DDR2 SDRAM operation.

A simplified version of the Command State Machine is shown in Figure 8. For readability, only the major state transitions are shown.

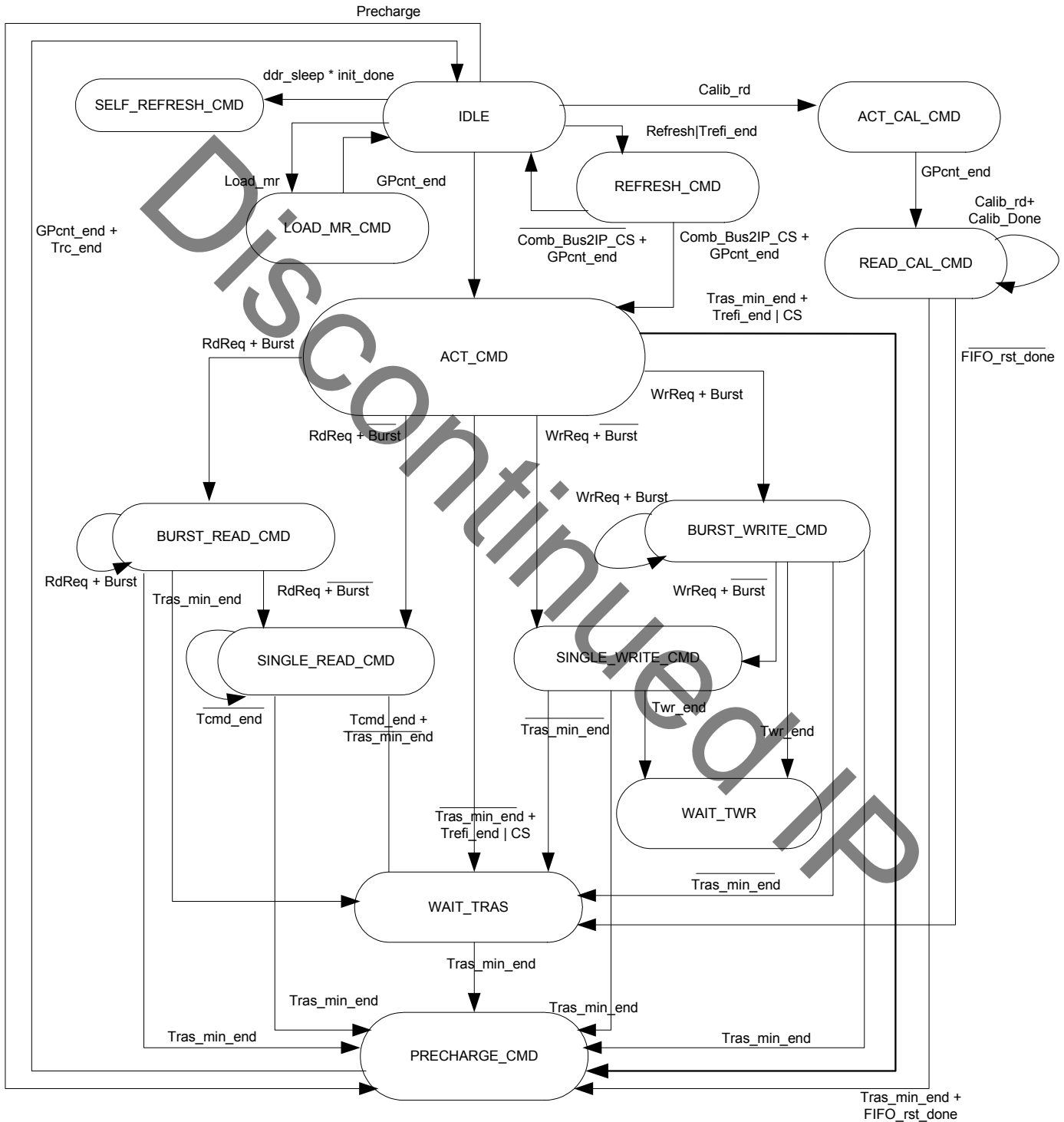


Figure 8: Command State Machine

Data State Machine

The Data State Machine is responsible for controlling the flow of data to and from the DDR2 SDRAM. The Data State Machine monitors the `pend_read` or `pend_write` signals from the Command State Machine to determine if more data transmissions are necessary. The Data State Machine waits for `C_DDR_CAS_LAT` during read operations and asserts the `ddr_brst_end` signal when the DDR2 SDRAM has completed the data transfer. The Data State Machine provides the `read_data_en` signal to the input DDR registers of an FPGA and Read Data Path FIFO. A simplified version of the Data State Machine is shown in **Figure 9**.

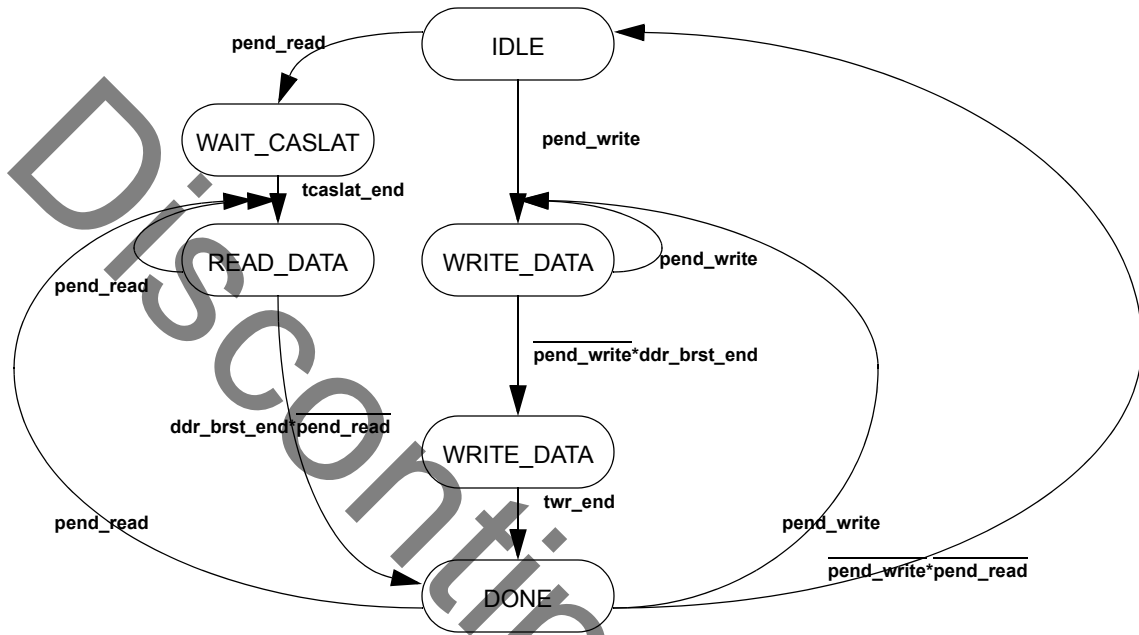


Figure 9: Data State Machine

Write Async FIFO and FIFO Read Control

This core requires the OPB or MCH logic to operate at a separate clock frequency than the DDR2 SDRAM interface. The parameter, `C_DDR_ASYNC_SUPPORT` is set to the constant value of 1 to allow the user to separate the system and DDR2 device clock domains. The `MCH_OPB_Clk` is used for writing in to the Async FIFO and the `DDR2 Device_Clk` is used for reading the data from the FIFO. The logic includes a state machine and an asynchronous FIFO in order to synchronize the command, data, address, data mask and control signals. The logic in this module is shown in **Figure 10** which includes state machine logic as well as instantiation of multiple asynchronous FIFOs. The output of the asynchronous FIFO is then provided in to the IO reg module.

The Command FIFO write enable signal (`cmd_fifo_wr_en`) is asserted when a DDR2 SDRAM command (Active, Write, Read, Refresh, Precharge) is issued by the Command State Machine. The control signal `dq_oe_cmb` enables writing of data and commands to the Data FIFO and Command FIFO, respectively. Reading of both the Command FIFO and the Data FIFO is controlled by the FIFO Read Control module. The FIFO Read Control module monitors the empty flags of Command FIFO and Data FIFO to enable reading each FIFO.

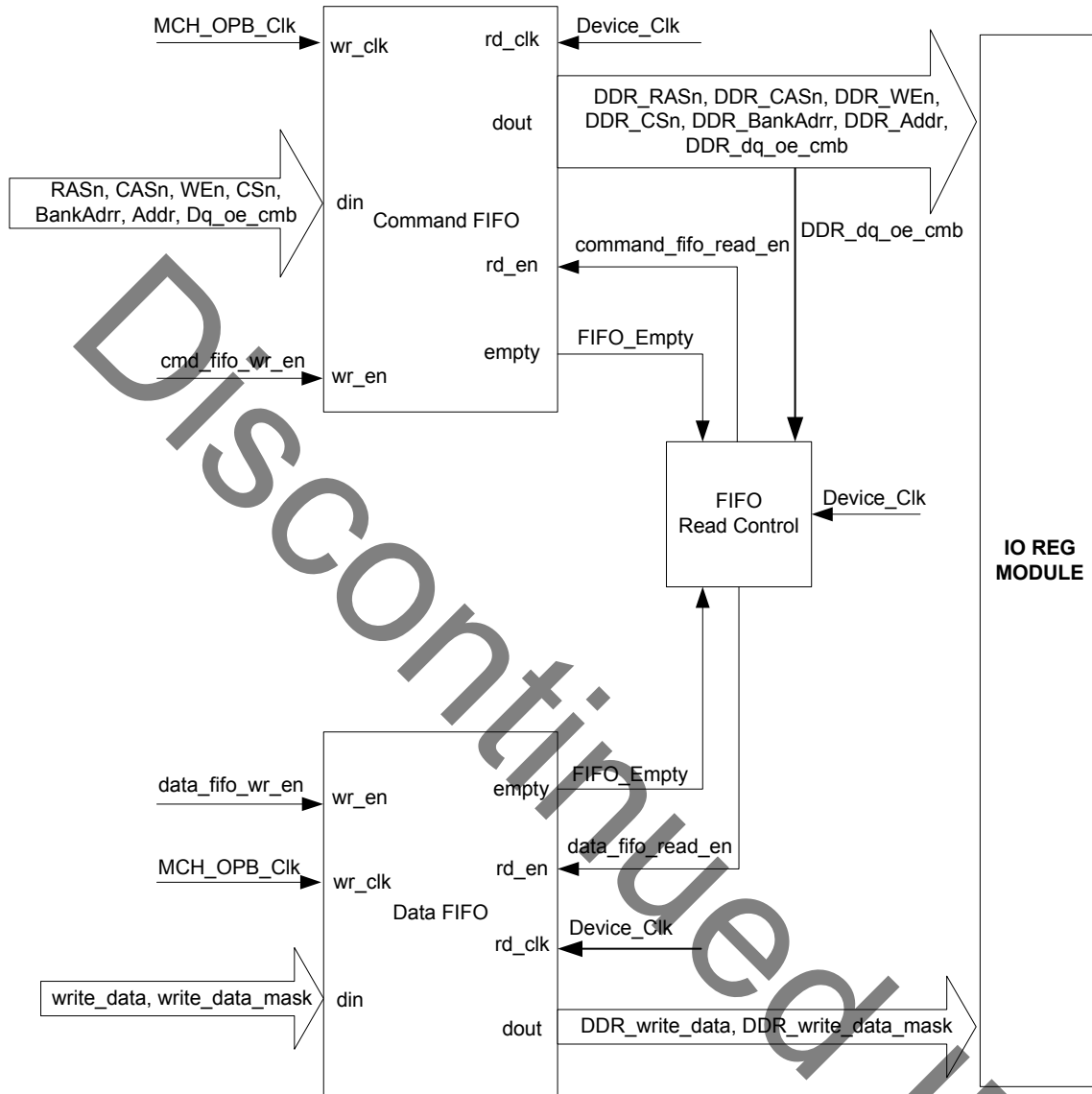


Figure 10: Block Diagram of Write Path Asynchronous Logic

Tap Control and Data Tap Increment

The Tap Control and Data Tap Increment modules (shown in Figure 12) are only instantiated when targeting Virtex-4 architectures (C_FAMILY = virtex4). Non Virtex-4 implementations do not instantiate these modules. The IDELAY module instantiation on all DQ and DQS signals is shown in Figure 22.

The Tap Control module issues back to back read cycles to the memory during the initialization sequence. During these read cycles, the incoming DQS signal(s) are sampled and the midpoint of the pulse is determined.

Once the midpoint/tap value is determined for the DQS signal(s), the Data Tap Increment module also sets the IDELAY tap value of the corresponding DQ data bits to the same value.

The IDELAY modules (in the IOB) are calibrated at an incremental value determined by the clock input to the IDELAYCTRL module(s). In this design, a 200 MHz clock is applied to the IDELAYCTRL module(s), which in turn set the time delay of the 64 count tap value.

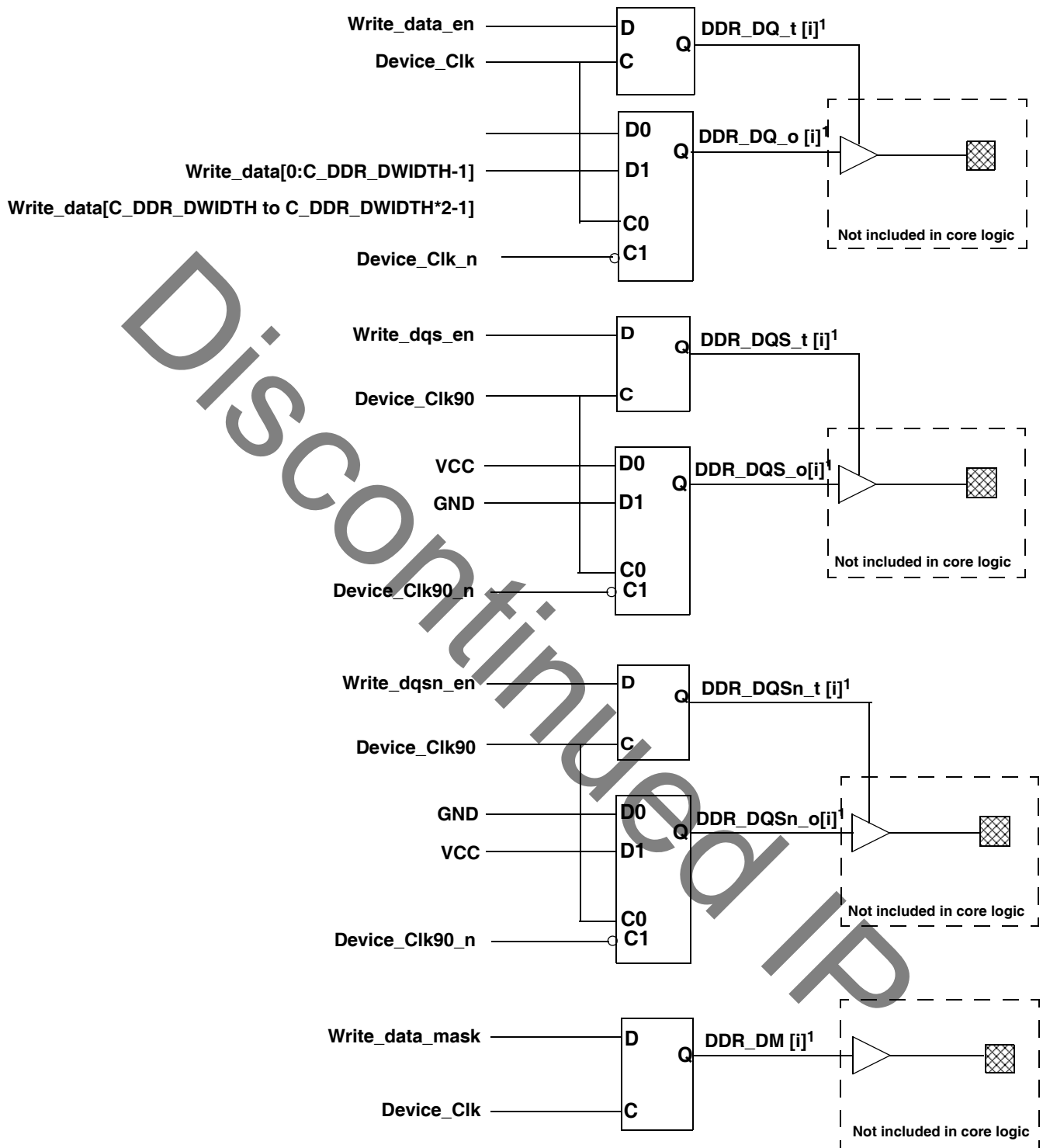
I/O Registers

Control Signals

All control signals and the address bus to the DDR2 SDRAM are registered in the IOBs of the FPGA.

Write Data

The DDR I/O registers are used to output the write data to the DDR2 SDRAM as shown in Figure 11. Since the DDR2 clocks (DDR_Clk and DDR_Clk_n) are generated from the Clk90 output of the DCM, the CLK0 output of the DCM is used to clock out the data so that the DDR2 clock is centered on the DDR2 SDRAM data.



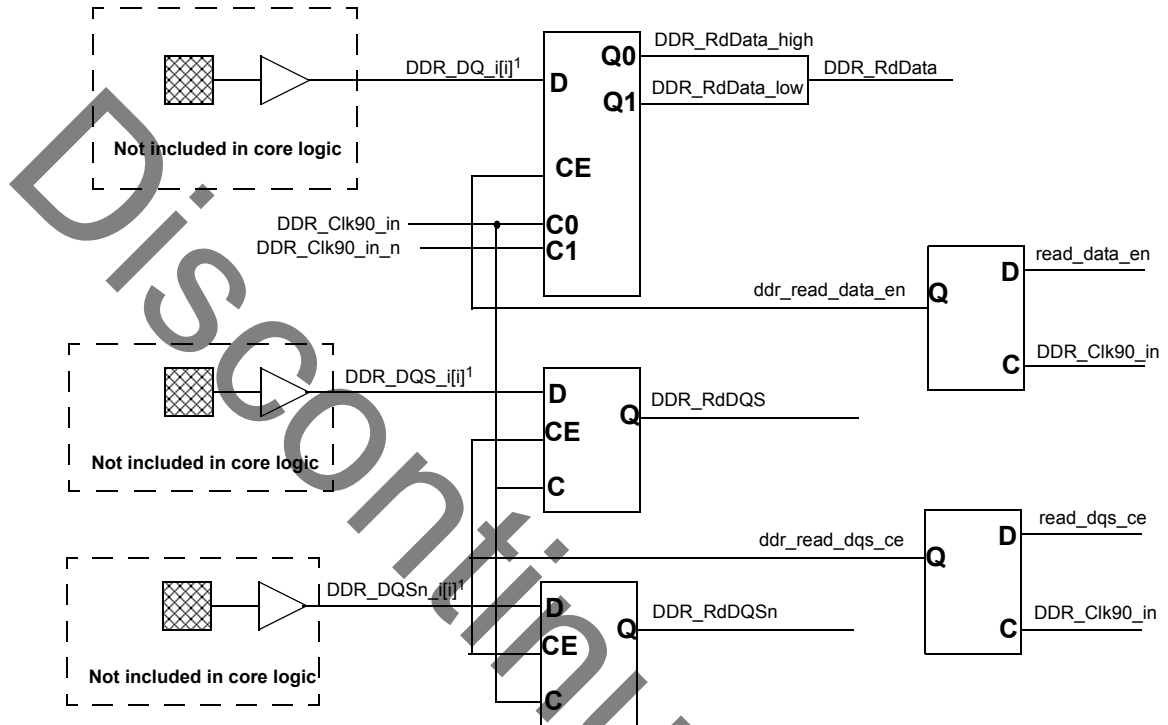
Note1: Signals are duplicated based on the parameter C_DDR_DWIDTH.

Figure 11: Write Data Path

Read Data (Non Virtex-4 Implementation)

The DDR I/O registers sample the read data from the DDR2 SDRAM as shown in Figure 12. The clock output (DDR_Clk) is used to supply the feedback clock (matching trace lengths) back into the FPGA. This feedback clock is fed into a DCM and generates DDR_Clk90_in and DDR_Clk90_in_n. These clock signals are used to capture the read data at the IOB during a read cycle as shown in Figure 12.

During a read cycle, the data strobe signal from the DDR2 SDRAM (DDR_DQS) is registered only on the rising edge of DDR_Clk90_in so that it is always high while the DDR2 SDRAM is transmitting data. This signal will be used by the Read Data Path logic as the write enable into a FIFO.

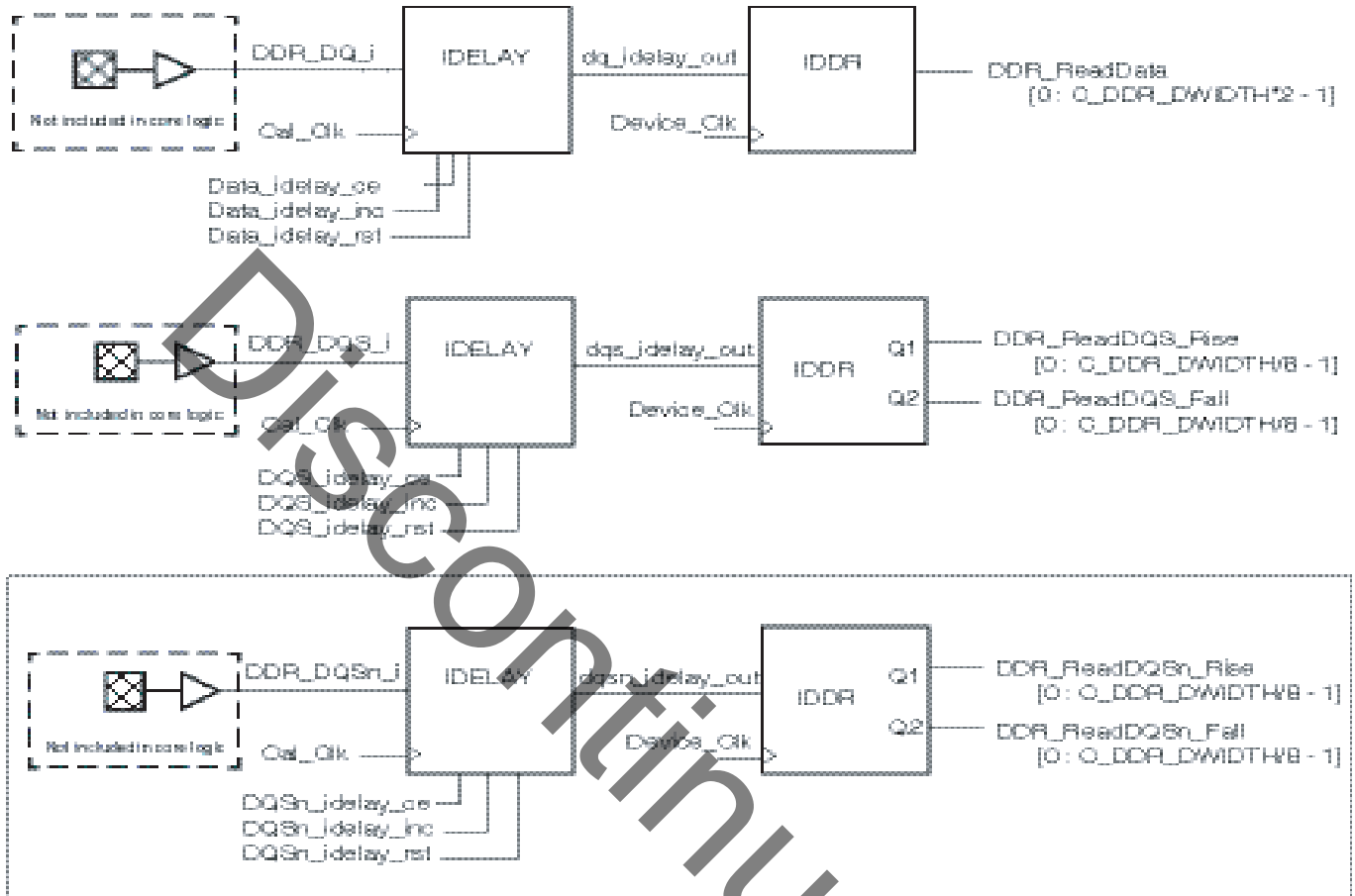


Note1: Signals are duplicated based on the parameter C_DDR_DWIDTH.

Figure 12: DDR2 Input Data Registers

Read Data (Virtex-4 Implementation)

The IOB IDELAY components and IDDR registers are used to read data from the DDR2 SDRAM as shown in Figure 13. The IDELAY modules are calibrated during the initialization sequence to center align the input DQ and DQS signals to the Device_Clk. The calibration determines the appropriate sample time based on Tsu and Th requirements on the IDDR register components.



Note:

1. `DDR_DQS_n` IOB is only instantiated when `C_DDR_ENABLE_DIFF_DQS = 1`.

Figure 13: V4 IDDR Register Usage

Read Data Path Logic

The read data output from the IOB will be a vector of size $C_DDR_DWIDTH * 2$ when applied as an input to the Read Data Path module.

The Read Data Path logic consists of an asynchronous FIFO in which the DDR2 SDRAM data is written on the rising edge of the Clk_DDR_Rddata (derived from DDR_Clk90_in , the DCM CLK90 output from the DDR feedback clock for non Virtex4 implementations) clock and read on the rising edge of MCH OPB clock. For Virtex-4 design implementations, the FIFO write clock is the rising edge of the $Device_Clk$, the same clock used to capture data in the IOB IDDR register components.

The asynchronous FIFO width is $C_DDR_DWIDTH * 2$. Once the FIFO is not empty, the data is read from the FIFO and a read acknowledge is generated. The asynchronous FIFO of the Read Data Path module is shown in [Figure 14](#).

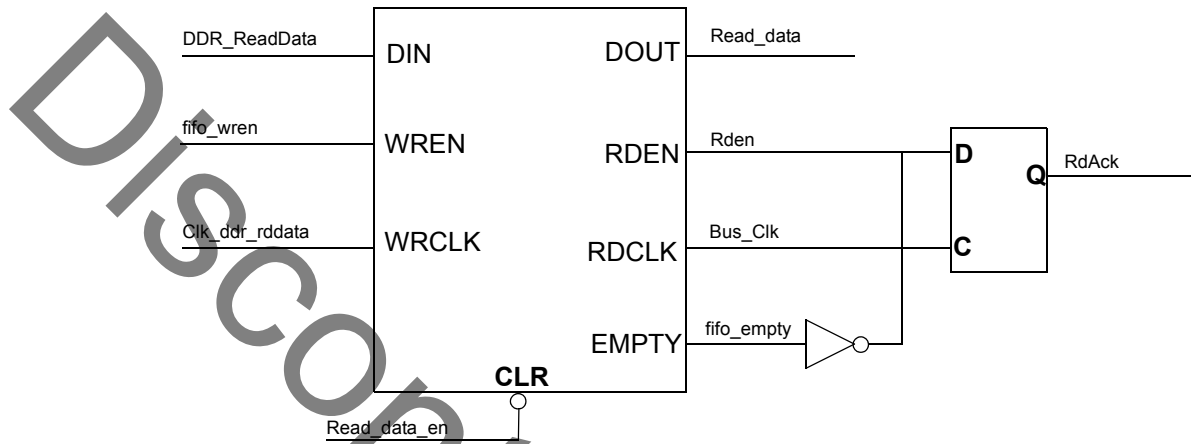


Figure 14: Read Data Path Module for Non Virtex-4 Architecture

The asynchronous FIFO of the Read Data Path module for Virtex-4 implementation is shown in [Figure 15](#).

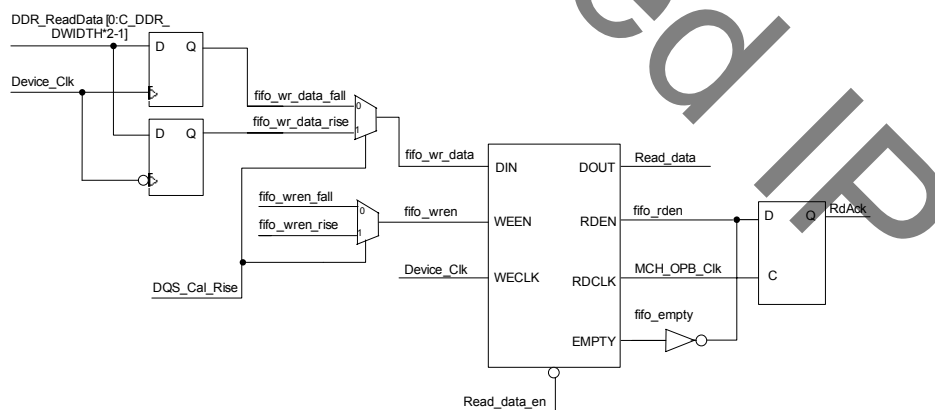


Figure 15: Read Data Path Module for Virtex-4 Architecture

Multiple Data Width

The Multiple Data Width module is instantiated when the data width of the DDR memory is equal to or greater than the data width of the OPB or MCH channels. In this controller, the Multiple Data Width module will be instantiated when the $C_DDR_DWIDTH = 32$ or $C_DDR_DWIDTH = 64$.

On Die Termination (ODT)

Termination resistance can be enabled on the DDR2 SDRAM memory devices. ODT allows selectable effective resistance (R_{tt} (effective)) to be enabled or disabled on a per transaction basis.

The ODT feature minimizes signal reflections in addition to the termination available in the FPGA IO buffers.

The MCH OPB DDR2 Controller signal, DDR_ODT , allows the controller to independently turn on or off the termination resistance internal to the DDR2 memory devices.

The impedance value of On Die Termination effective resistance (R_{tt}) can be selected using the parameter $C_DDR2_ODT_SETTING$ described in [Table 1](#) as "ODT not selected" or "ODT selected (75Ω or 150Ω)". R_{tt} values are set during DDR2 SDRAM initialization process using the Extended Mode Register (EMRS1) by the controller based on the parameter setting. [Figure 16](#) shows the ODT structure.

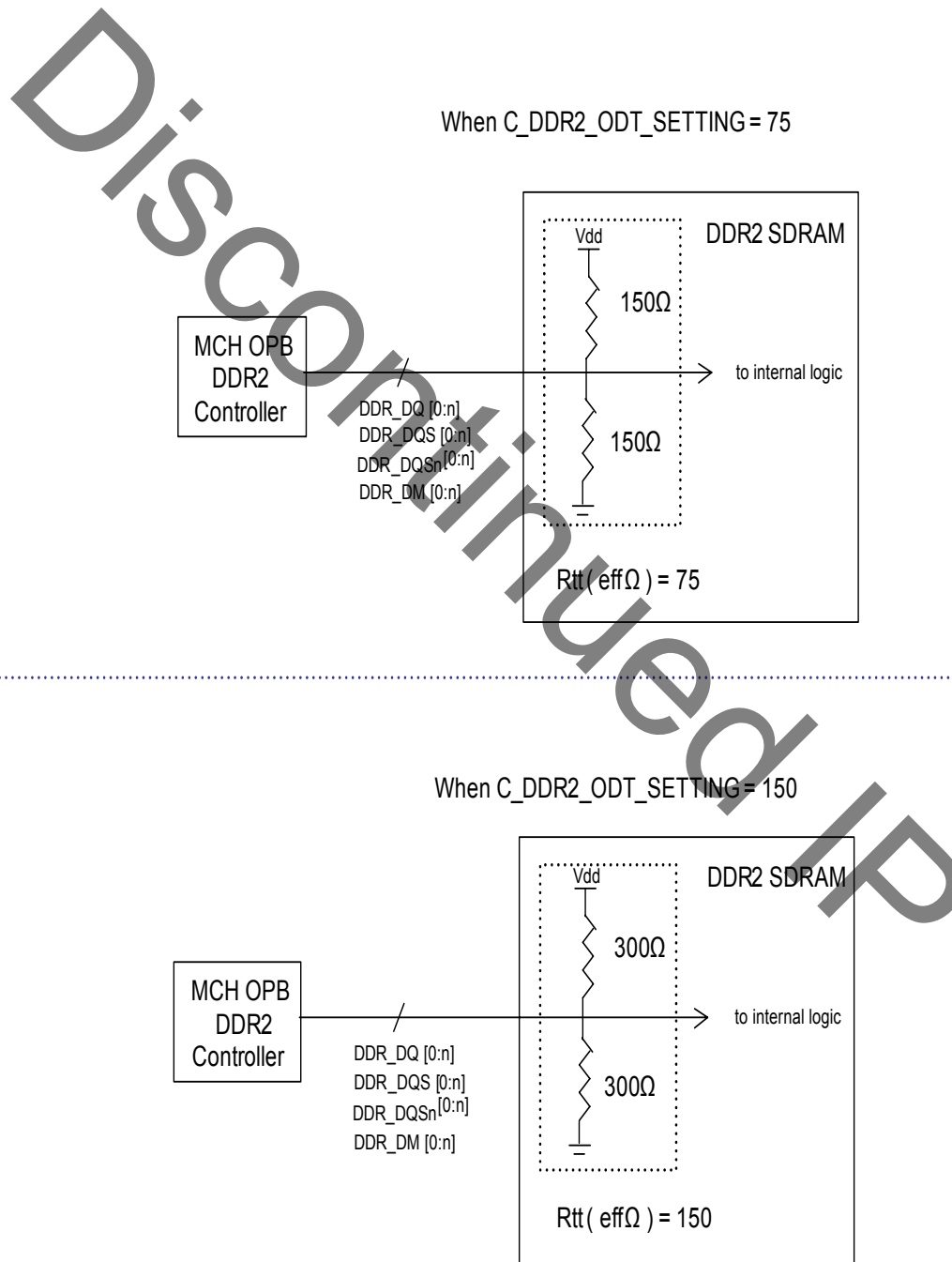


Figure 16: ODT Structure

Figure 17 shows the ODT turn-on delay, tAOND and turn-off delay, tAOFD timing. When ODT is enabled it will be active for all memory transactions. The ODT pin will be asserted (equal to '1') tAOND before the data is active on the data pins and ODT will be disabled (equal to '0') once tAOFD is met.

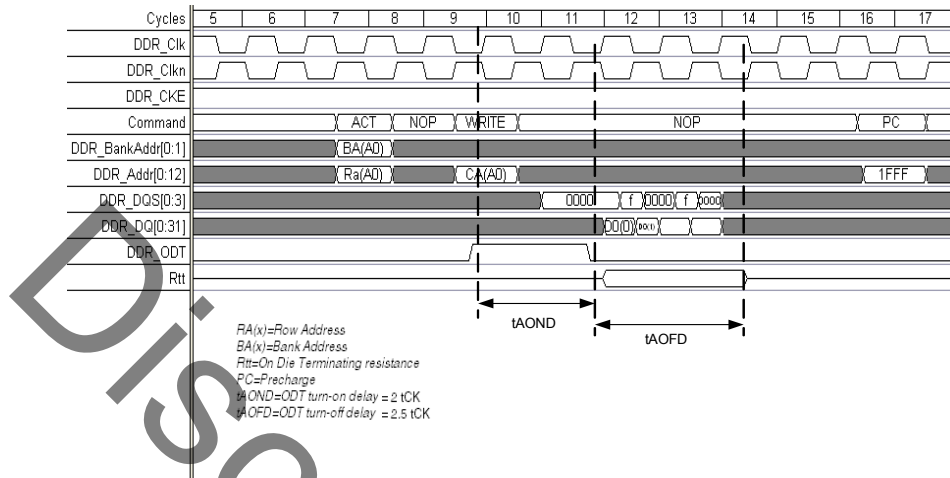


Figure 17: ODT Timing

Differential DQS

DDR2 SDRAM supports an additional differential data strobe, DQSn. Differential DQS is enabled by the Initialization State Machine in writing to the Extended Mode Register of the DDR2 SDRAM memory (when C_DDR_ENABLE_DIFF_DQS = 1). If differential strobes are enabled, DQS operates the same as in single-ended mode with the addition of DQSn operating as the complement of DQS.

Since the DQS signal behavior is source-synchronous, during read operations the DDR2 SDRAM will drive both the DQS and DQSn signals, if differential DQS is enabled. During write operations, the MCH OPB DDR2 controller will drive the DQS and DQSn.

The DQS and DQSn signals are designed as two independent I/O signals to the DDR2 memory, a differential IO buffer in the FPGA is not required.

DDR2 Clocking

MCH OPB DDR2 SDRAM Clocking

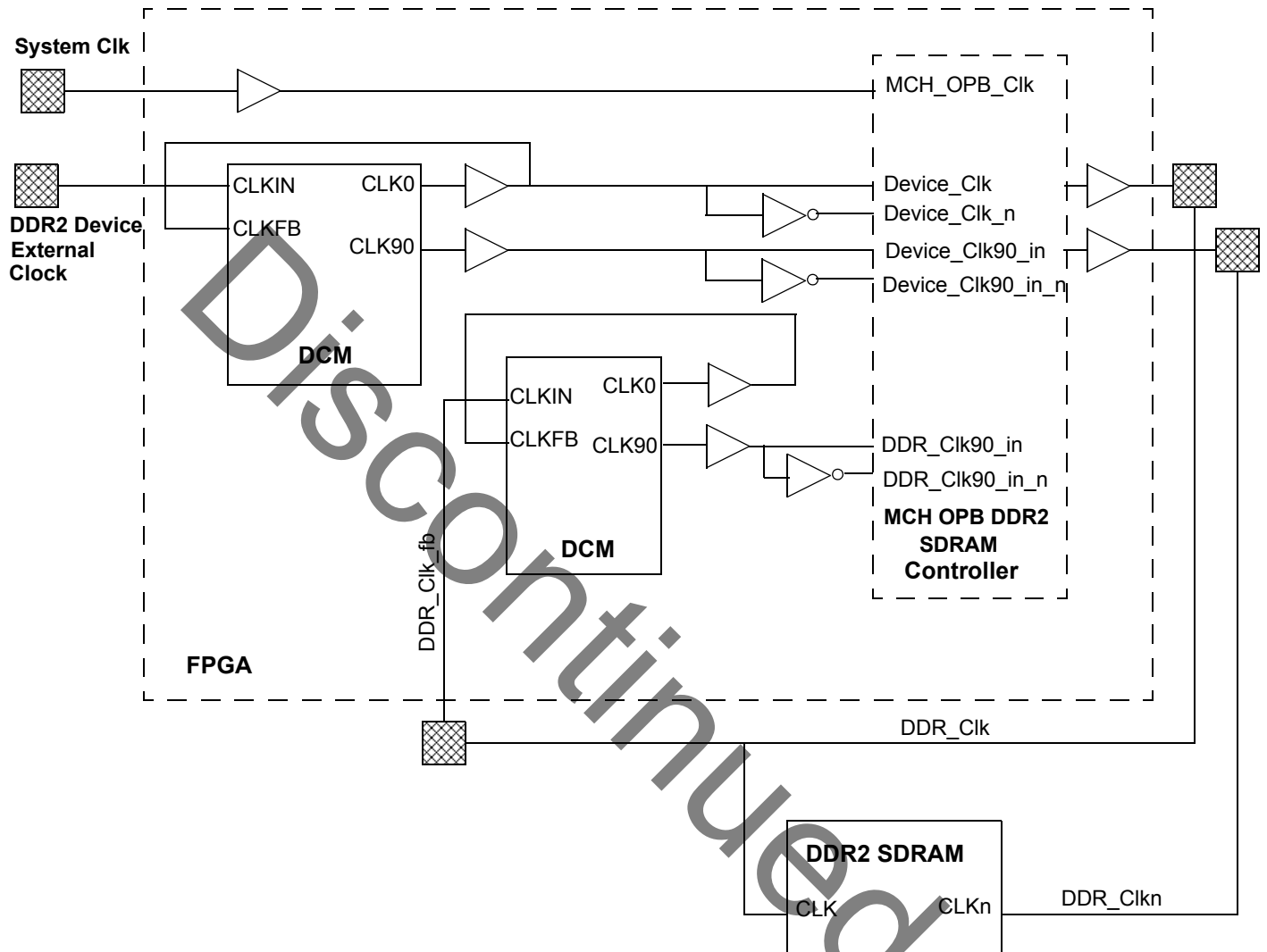
Table 12 shows the clock frequency combinations supported in the MCH OPB DDR2 SDRAM controller for the MCH/OPB bus and the DDR2 SDRAM clock.

Table 12: Supported Clocking Configurations

C_MCH_OPB_CLK_PERIOD_PS	C_DDR_CLK_PERIOD_PS
15000 ps (66 MHz)	7500 ps (133 MHz)
10000 ps (100 MHz)	7500 ps (133 MHz)
10000 ps (100 MHz)	5000 ps (200 MHz)

Non Virtex-4 Clock Generation

The clocking scheme required in the FPGA (for the design implementations other than Virtex-4) and used by the MCH OPB DDR2 SDRAM controller is shown in Figure 18 and Figure 19.

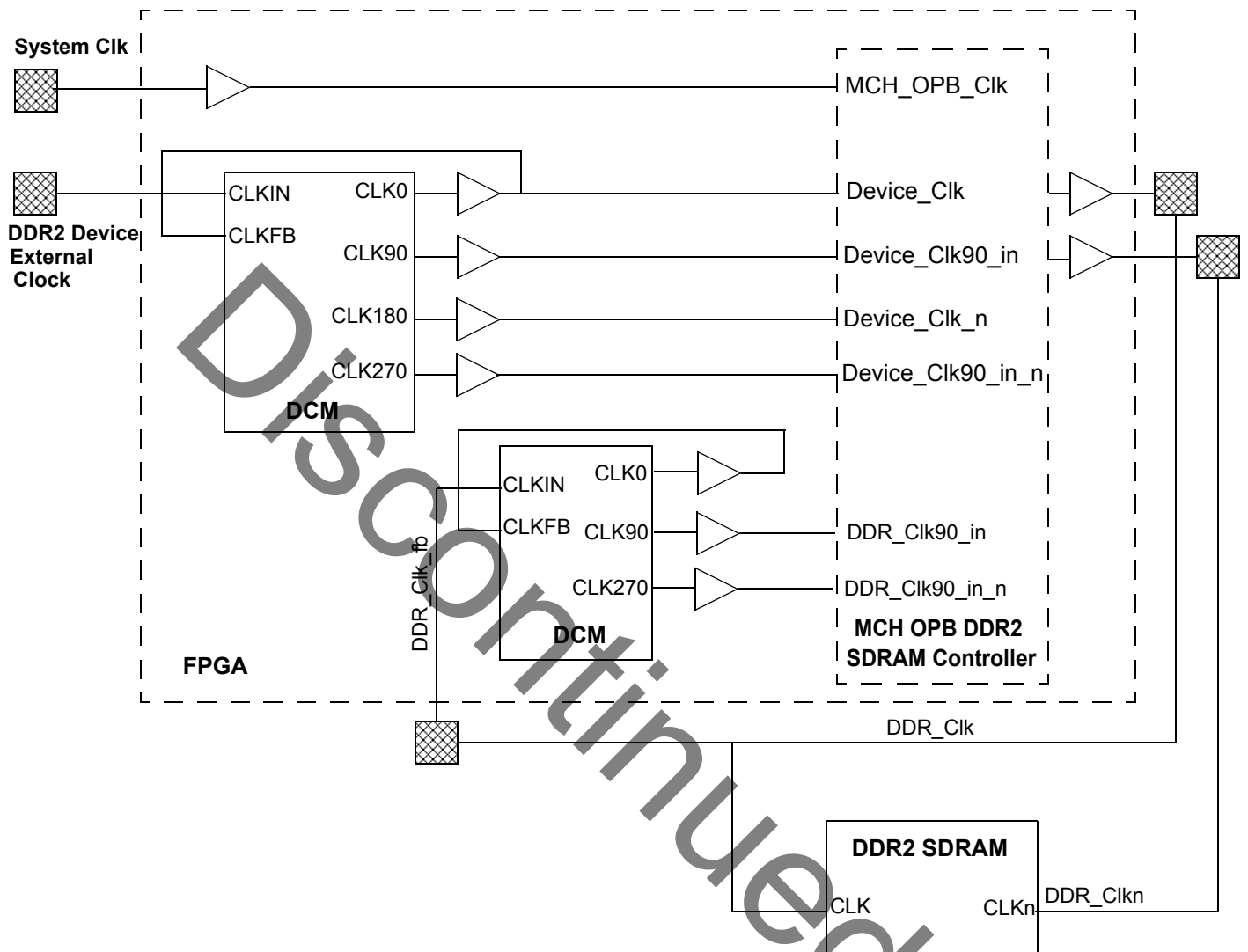


Note 1: This clocking configuration uses local clock inversion for the generation of Device_Clk_n, Device_Clk90_in_n, & DDR_Clk90_in_n.

Note 2: An additional BUFG is used for the MCH_OPB_Clk in this configuration.

Note 3: A total of 5 BUFGs are used in this configuration.

Figure 18: MCH OPB DDR2 SDRAM Controller - Non-Virtex-4 Clocking (Option 1)



Note 1: This clocking configuration uses global clock inversion for the generation of Device_Clk_n, Device_Clk90_in_n & DDR_Clk90_in_n.

Note 2: An additional BUFG is used for the MCH_OPB_Clk in this configuration.

Note 3: A total of 8 BUFGs are used in this configuration.

Figure 19: MCH OPB DDR2 SDRAM Controller - Non-Virtex-4 Clocking (Option 2)

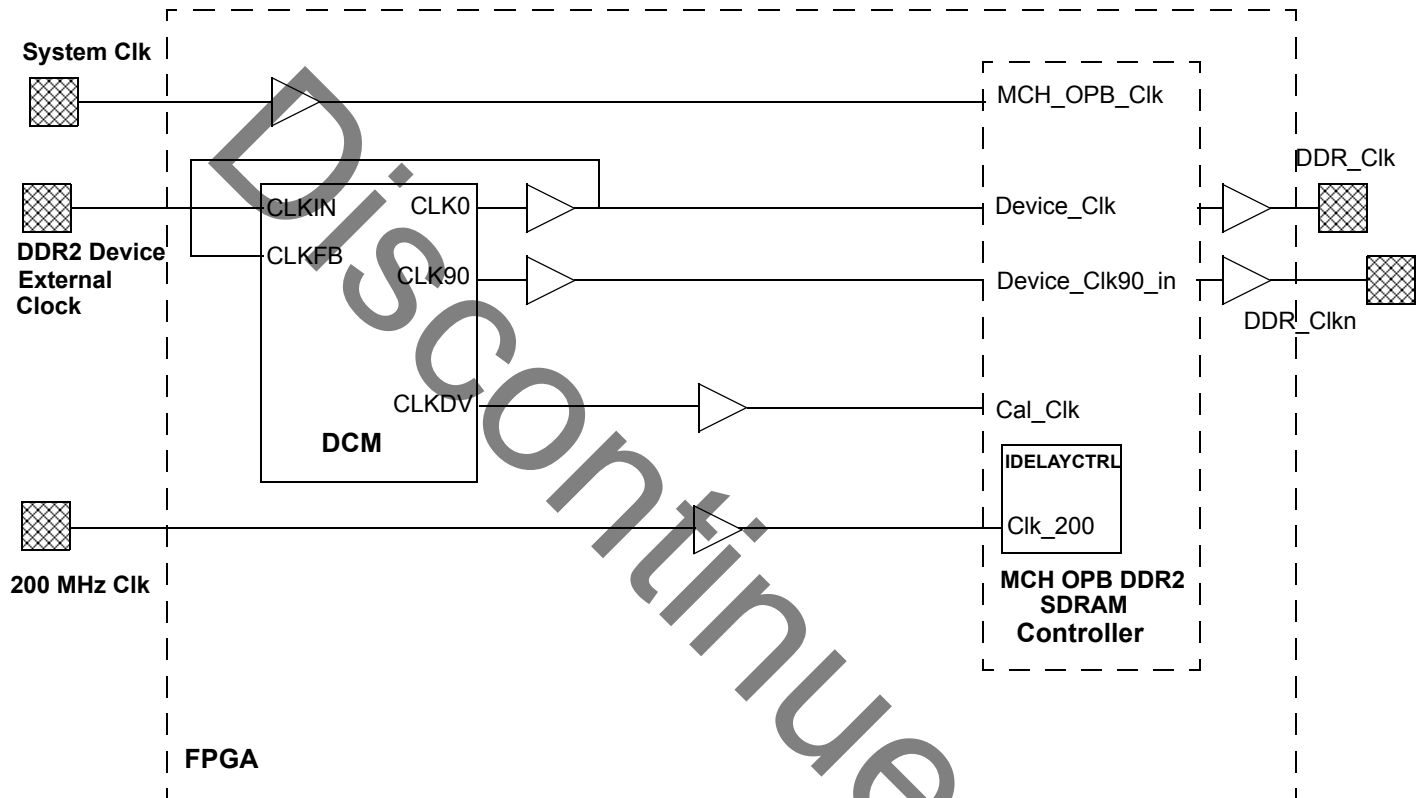
DDR2 SDRAM Clock Input Synchronization

For design implementations other than Virtex-4, a DCM is required for the DDR feedback clock, DDR_Clk_FB. The DCM on the feedback clock is used to create a clock pair that is center aligned with the DQ signals during a read cycle. The DDR_Clk output shown in Figure 18 will need to be connected to the DDR_Clk_fb shown in Figure 19 as an external board connection. The CLK90 output of the DDR_Clk_FB DCM is used by the MCH OPB DDR2 SDRAM core to register the data (DQ) during a read cycle.

Due to the variance in board layout, and timing on the DDR_DQ & DDR_DQS signals, the phase shifting on the DDR_Clk_FB should be analyzed.

Virtex-4 Clock Generation

The clocking scheme required in the FPGA for the design implementations targeting for Virtex-4 and used by the MCH OPB DDR2 SDRAM controller are shown in Figure 20.



Note 1: An additional BUFG is used for the MCH_OPB_Clk in this configuration.

Note 2: A total of 5 BUFGs are used in this configuration.

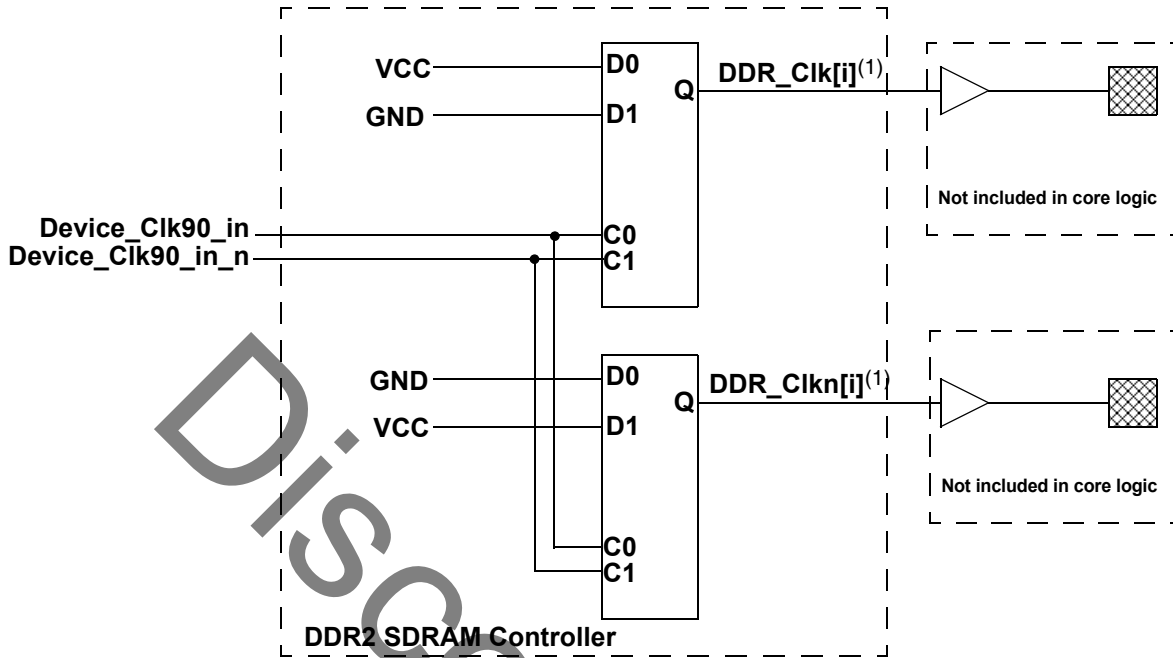
Figure 20: MCH OPB DDR2 controller - Virtex-4 Clocking

Controller Clock Inputs

A DCM is required to generate the clocks used by MCH OPB DDR2 SDRAM controller as shown in Figure 18 through Figure 20. A 90 degree and 270 degree phase shifted output of the DCM is a required input to the MCH OPB DDR2 SDRAM controller core. These are used to generate the DDR_Clk/DDR_Clk_n and DQS signals to DDR2 SDRAM. The inverted clock can be derived using local inversion (to minimize BUFG system resource usage) or use direct outputs of the DCM.

DDR2 Clock Generation

The clock output to the DDR2 SDRAM is generated using the DDR IOB registers as shown in Figure 21. The Device_Clk90_in is used to generate the DDR_Clk (and DDR_Clk_n) so that the clock is centered on the DQ signal to the DDR2 SDRAM.



Note 1: Duplicated based on parameter C_NUM_CLK_PAIRS.

Figure 21: DDR2 SDRAM Clock Generation

Timing Diagrams

XCL Protocol Cacheline Write Timing Diagrams

Figure 22 shows an XCL protocol channel performing a cacheline write on 32-bit DDR2 SDRAM.

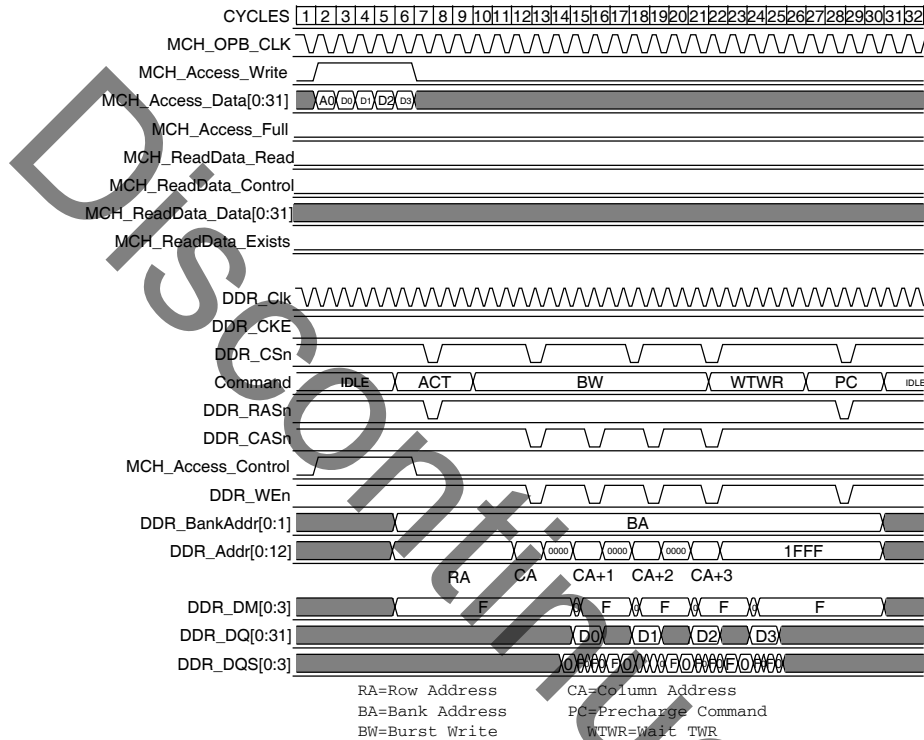


Figure 22: XCL Cacheline Write Operation With 32-Bit DDR2 SDRAM

XCL Protocol Cacheline Read Timing Diagrams

Figure 23 shows an XCL protocol channel performing a cacheline read on 32-bit DDR2 SDRAM.

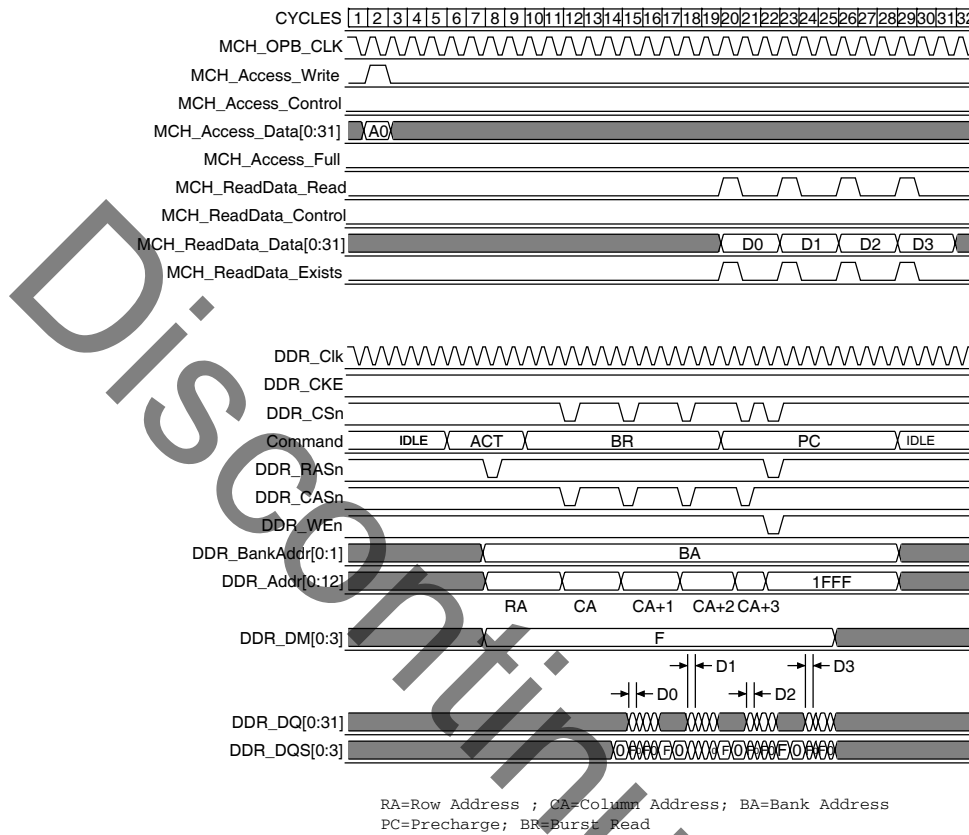


Figure 23: XCL Cacheline Read Operation With 32-Bit DDR2 SDRAM

XCL Protocol Single Write Timing Diagrams

Figure 24 shows an XCL protocol channel performing a single write on 32-bit DDR2 SDRAM

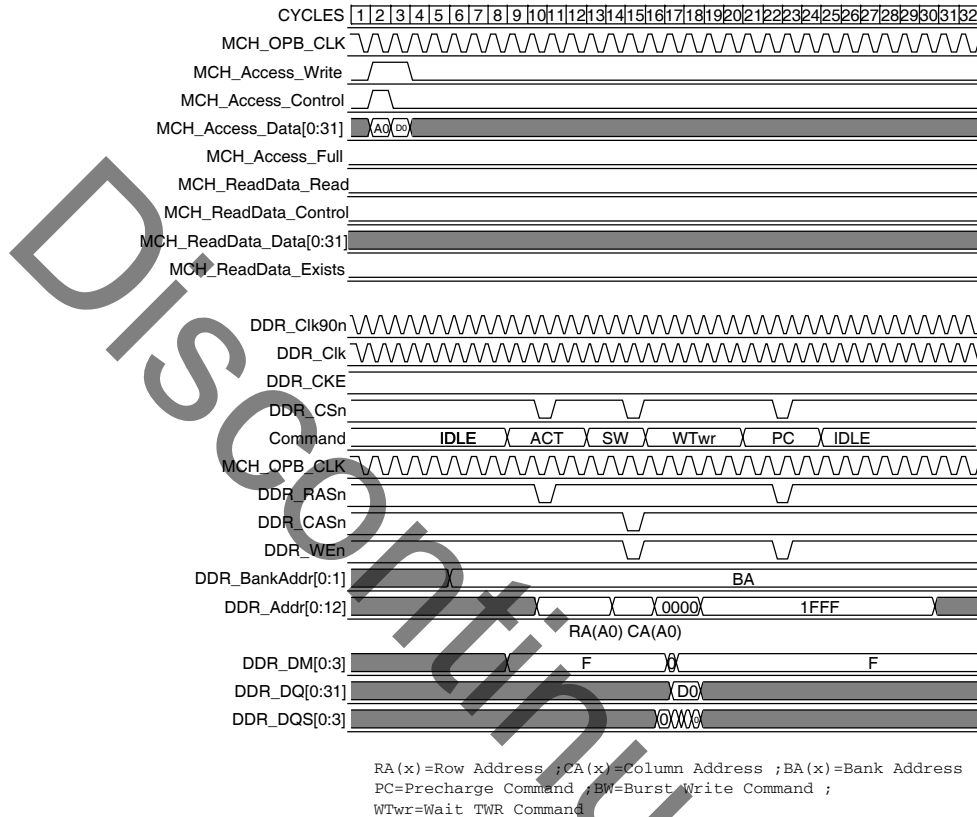


Figure 24: XCL Single Write Operation With 32-Bit DDR2 SDRAM

XCL Protocol Single Read Timing Diagrams

Figure 25 shows an XCL protocol channel performing a single read on 32-bit DDR2 SDRAM

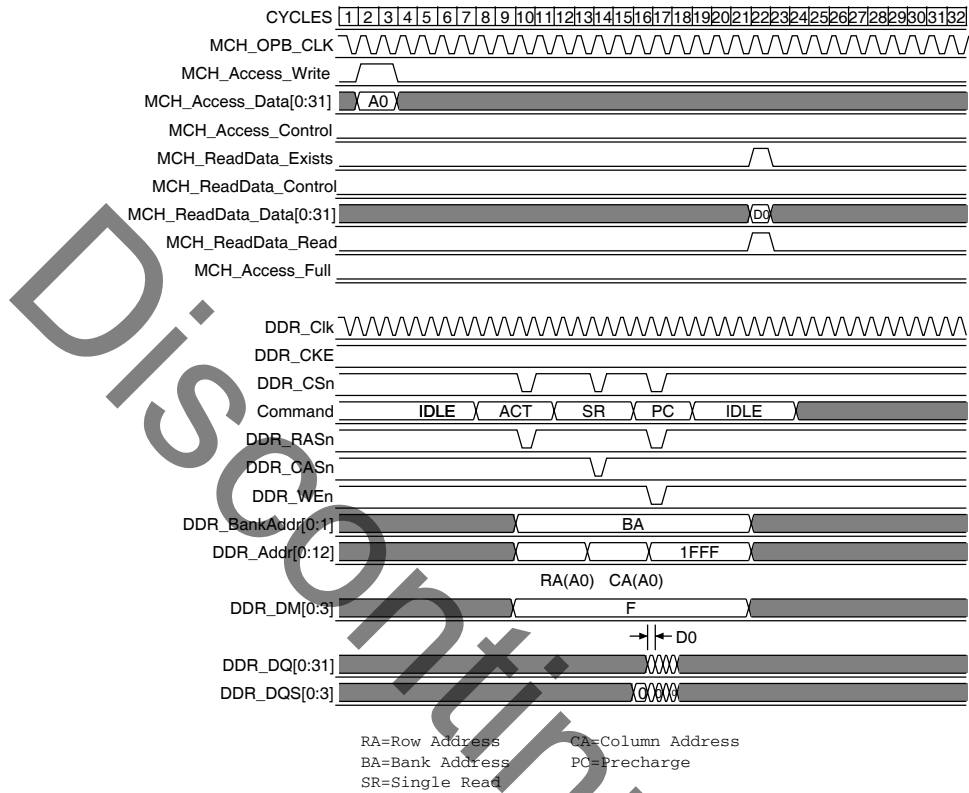


Figure 25: XCL Single Read Operation With 32-Bit DDR2 SDRAM

OPB Burst Write Timing Diagrams

Figure 26 shows an OPB burst write operation on 32-bit DDR2 SDRAM.

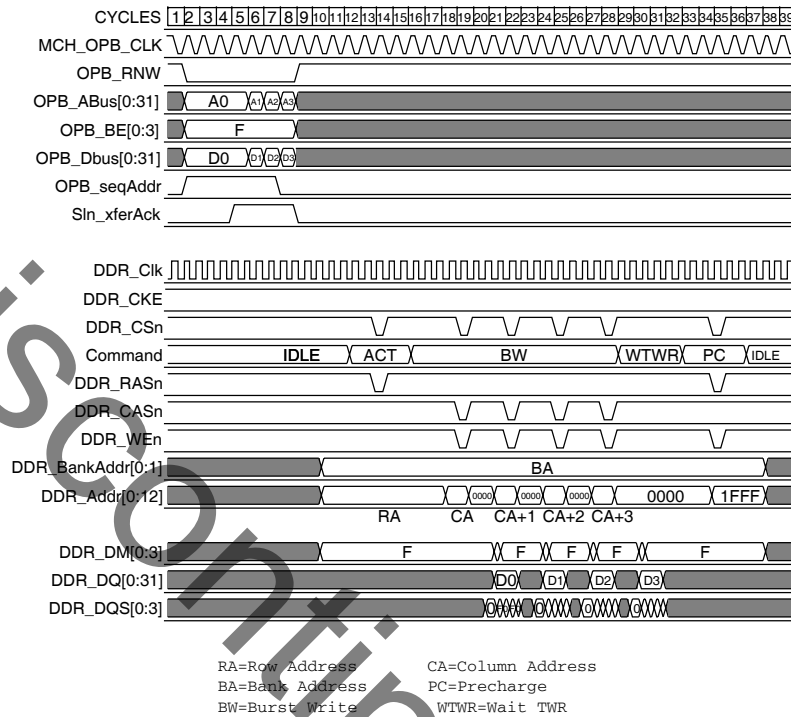


Figure 26: OPB Burst Write operation With 32-Bit DDR2 SDRAM

Figure 27 shows an OPB burst write operation on 16-bit DDR2 SDRAM.

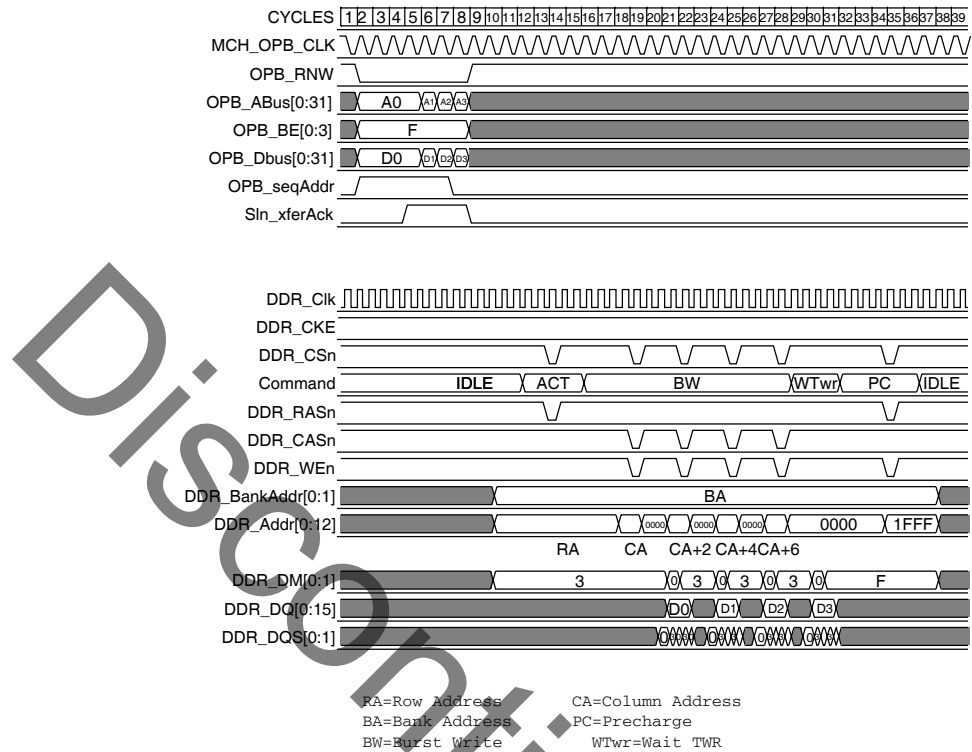


Figure 27: OPB Burst Write operation With 16-Bit DDR2 SDRAM

OPB Burst Read Timing Diagrams

Figure 28 shows an OPB burst read operation on 32-bit DDR2 SDRAM.

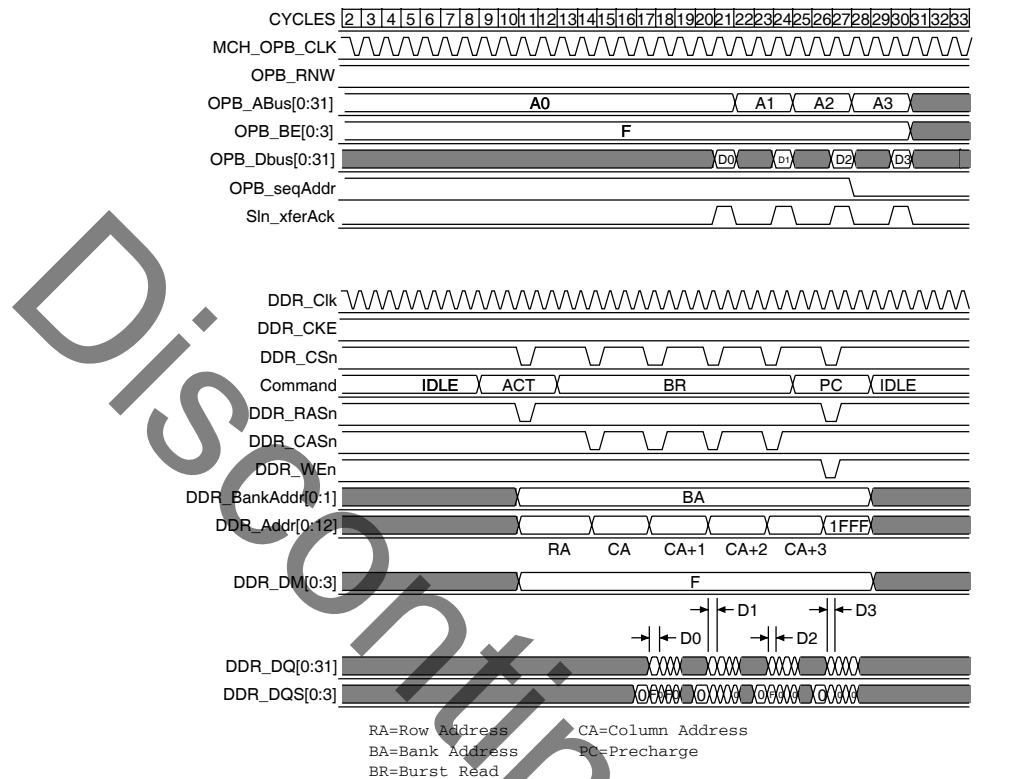


Figure 28: OPB Burst Read operation With 32-Bit DDR2 SDRAM

Figure 29 shows an OPB burst read operation on 16-bit DDR2 SDRAM.

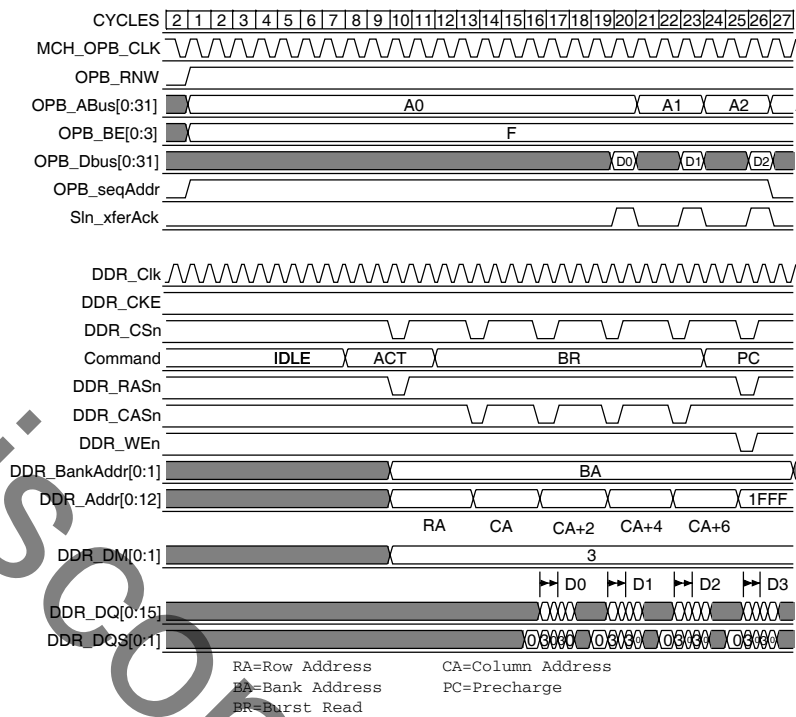


Figure 29: OPB Burst Read operation With 16-Bit DDR2 SDRAM

OPB Single Write Timing Diagrams

Figure 30 shows an OPB single write operation on 32-bit DDR2 SDRAM.

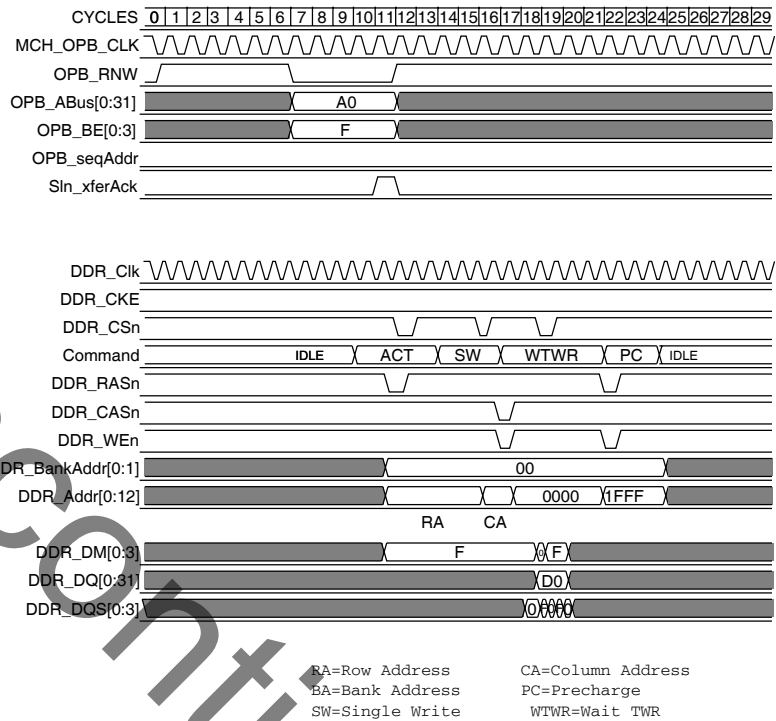


Figure 30: OPB Single Write operation With 32-Bit DDR2 SDRAM

OPB Single Read Timing Diagrams

Figure 31 shows an OPB single read operation on 32-bit DDR2 SDRAM.

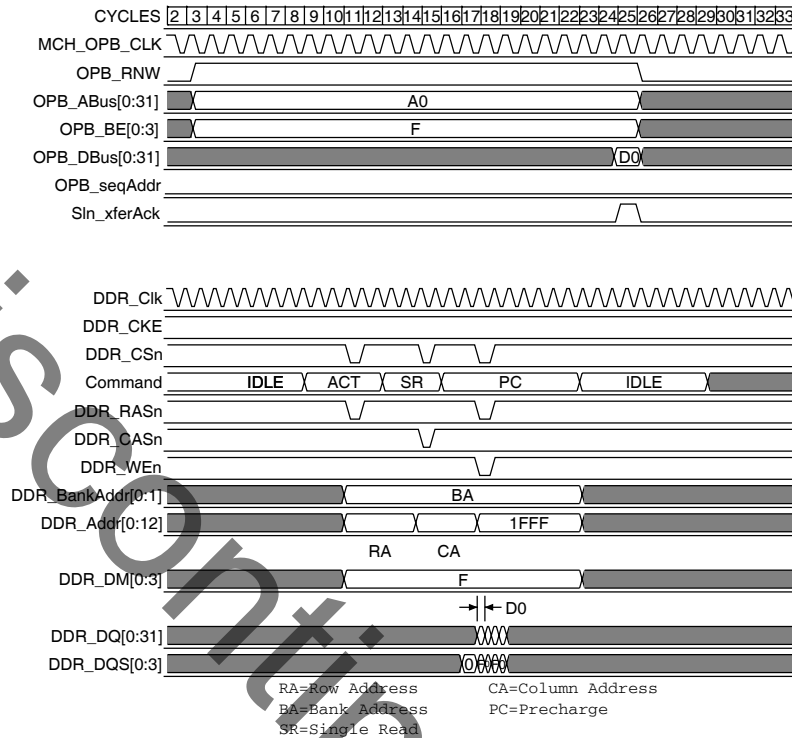


Figure 31: OPB Single Read operation With 32-Bit DDR2 SDRAM

Design Constraints

Note: An example UCF for this core is available and must be modified for use in the system. Please refer to the *EDK Getting Started Guide* for the location of this file.

Timing Constraints

For complete timing coverage, all clock inputs to the FPGA should be assigned a timing constraint. Using any of the recommended DCM configurations (for design implementations other than Virtex4) shown in [Figure 18 on page 32](#) or [Figure 19 on page 33](#), the ISE tools will derive all proper timing constraints for the DDR2 core. For design implementations other than Virtex-4, a timing constraint should be placed on the system clock input as well as the DDR clock feedback. An example for running the MCH and OPB at 100 MHz and the DDR2 clock at 133 MHz is shown in [Figure 32](#).

```

NET "MCH_OPB_Clk" TNM_NET = "MCH_OPB_Clk";
TIMESPEC "TS_MCH_OPB_Clk" = PERIOD "MCH_OPB_Clk" 10 ns HIGH 50%;

NET "Device_Clk" TNM_NET = "Device_Clk";
TIMESPEC "TS_Device_Clk" = PERIOD "Device_Clk" 7.5 ns HIGH 50%;

NET "DDR_Clk_fb" TNM_NET = "DDR_Clk_fb";
TIMESPEC "TS_DDR_Clk_fb" = PERIOD "DDR_Clk_fb" 7.5 ns HIGH 50%;

```

Figure 32: Non Virtex-4 Timing Constraints

For Virtex-4 design implementations using the recommended DCM setup shown in [Figure 20 on page 34](#), only the external clock inputs are required to be assigned a timing constraint. An example for a Virtex-4 implementation is shown in [Figure 33](#) where the MCH / OPB clock is running at 100 MHz and the DDR2 clock frequency is 133 MHz.

```

NET "MCH_OPB_Clk" TNM_NET = "MCH_OPB_Clk";
TIMESPEC "TS_MCH_OPB_Clk" = PERIOD "MCH_OPB_Clk" 10 ns HIGH 50%;

NET "Device_Clk" TNM_NET = "Device_Clk";
TIMESPEC "TS_Device_Clk" = PERIOD "Device_Clk" 7.5 ns HIGH 50%;

NET "Clk_200" TNM_NET = "Clk_200";
TIMESPEC "TS_Clk_200" = PERIOD "Clk_200" 5 ns HIGH 50%;

```

Figure 33: DDR2 Timing Constraints for Virtex4

Pin Constraints

The DDR2 SDRAM I/O should be set to the SSTL18 I/O standard. If external pullups/pulldowns are not available on the DDR2 SDRAM DQ and DQS signals, then these pins should be specified to use pullup or pulldown resistors. Pulldown resistors are preferred. An example is shown in [Figure 34](#).

```

NET DDR_Clk          IOSTANDARD = SSTL18_I;
NET DDR_Clkn         IOSTANDARD = SSTL18_I;
NET DDR_CKE          IOSTANDARD = SSTL18_I;
NET DDR_CSn          IOSTANDARD = SSTL18_I;
NET DDR_RASn         IOSTANDARD = SSTL18_I;
NET DDR_CASn         IOSTANDARD = SSTL18_I;
NET DDR_WEn          IOSTANDARD = SSTL18_I;
NET DDR_DM<*>       IOSTANDARD = SSTL18_I;
NET DDR_BankAddr<*> IOSTANDARD = SSTL18_I;
NET DDR_Addr<*>     IOSTANDARD = SSTL18_I;
NET DDR_DQ<*>       IOSTANDARD = SSTL18_II;
NET DDR_DQS<*>      IOSTANDARD = SSTL18_II;
NET DDR_DQSn<*>     IOSTANDARD = SSTL18_II;
NET DDR_ODT          IOSTANDARD = SSTL18_I;

```

Figure 34: MCH OPB DDR2 SDRAM Controller's Pin Constraints

IDELAY Constraints

For Virtex-4 design implementations the use of the IDELAY in the IOB modules is required. With using any IDELAY components within the FPGA, an IDELAYCTRL module is necessary. The IDELAYCTRL module provides the necessary tap increments for each IDELAY module to which it is associated.

In the ISE tools, if only one IDELAYCTRL module is instantiated and the DDR2 SDRAM signal pin assignments are across multiple clock regions, the tools will replicate the IDELAYCTRL module. To prevent the tools from duplicating the IDELAYCTRL to all locations on the FPGA, the user must specify how many IDELAYCTRL modules are needed. This is specified with

the C_NUM_IDELAYCTRL design parameter. It is the responsibility of the designer to location constrain each IDELAYCTRL based on the clock regions where IOB DDR2 SDRAM IOB signals reside.

For instance, if C_NUM_IDELAYCTRL = 4, then the user must add UCF constraints to location constrain these modules, as shown in [Figure 35](#).

```
INST mch_opb_ddr2_0/*/IDELAYCTRL_I0 LOC=IDELAYCTRL_XnYm;  
INST mch_opb_ddr2_0/*/IDELAYCTRL_I1 LOC=IDELAYCTRL_XnYm;  
INST mch_opb_ddr2_0/*/IDELAYCTRL_I2 LOC=IDELAYCTRL_XnYm;  
INST mch_opb_ddr2_0/*/IDELAYCTRL_I3 LOC=IDELAYCTRL_XnYm;
```

Figure 35: Virtex-4 IDELAY Constraints

Design Implementation

Target Technology

The intended target technology is Spartan-3, Virtex-II Pro and Virtex-4 family FPGAs.

Device Utilization and Performance Benchmarks

The MCH OPB DDR2 SDRAM controller is a module that will be used with other design pieces in the FPGA, the utilization and timing numbers reported in this section are estimates. As the MCH OPB DDR2 SDRAM controller is combined with other pieces of the FPGA design, the utilization of FPGA resources and timing of the MCH OPB DDR2 SDRAM controller design will vary from the results reported here. The MCH OPB DDR2 SDRAM controller benchmarks are shown in [Table 13](#), [Table 14](#) and [Table 15](#) for a Spartan-3 (xc3s2000), Virtex-II Pro (xc2vp20) and Virtex-4 (xc4vlx40) FPGAs.

Table 13: Performance and Resource Utilization (Spartan-3)

Parameter Values						Device Resources			Performance	
C_NUM_CHANNELS	C_INCLUDE_OPB_IPIF	C_INCLUDE_OPB_BURST_SUPPORT	C_REG_DIMM	C_NUM_BANKS_MEM	C_DDR_DWIDTH	Slices	Slice FFs	4-input LUTs	MCH/OPB Clock Fmax (MHz)	DDR2 Device Clock Fmax (MHz)
1	1	0	0	1	16	800	572	868	81	139
1	0	0	0	4	16	819	579	867	76	136
4	0	0	0	1	16	1465	916	1747	69	139
2	1	0	0	1	16	1304	883	1391	70	138
2	1	1	0	1	16	1353	916	1609	70	141
4	1	1	0	1	16	1705	1108	2094	69	136
2	1	1	0	2	16	1366	898	1650	69	143
2	1	0	0	2	16	1308	888	1446	69	135
4	1	1	0	4	16	1767	1122	2210	68	135
2	1	1	1	1	16	1434	972	1613	70	138
4	1	1	1	1	16	1726	1164	2098	68	136
2	1	1	1	2	16	1449	954	1654	70	137
2	1	0	1	2	16	1309	944	1450	70	134
4	1	1	1	4	16	1789	1178	2214	68	137
1	1	0	0	1	32	969	704	962	79	136
1	0	0	0	4	32	962	711	932	79	135
4	0	0	0	1	32	1616	1058	1829	68	133
2	1	0	0	1	32	1387	1017	1463	69	133
2	1	1	0	1	32	1498	1215	1676	68	134
4	1	1	0	1	32	1889	1246	2218	68	135
2	1	1	0	2	32	1489	1036	1740	68	134
2	1	0	0	2	32	1439	1021	1505	68	134
4	1	1	0	4	32	1939	1268	2322	68	135
2	1	1	1	1	32	1537	1167	1680	68	136
4	1	1	1	1	32	1975	1367	2222	67	141
2	1	1	1	2	32	1617	1155	1744	69	136

Table 13: Performance and Resource Utilization (Spartan-3)

Parameter Values						Device Resources			Performance	
C_NUM_CHANNELS	C_INCLUDE_OPB_IPIF	C_INCLUDE_OPB_BURST_SUPPORT	C_REG_DIMM	C_NUM_BANKS_MEM	C_DDR_DWIDTH	Slices	Slice FFs	4-input LUTs	MCH/OPB Clock Fmax (MHz)	DDR2 Device Clock Fmax (MHz)
2	1	0	1	2	32	1531	1140	1509	69	134
4	1	1	1	4	32	2032	1382	2327	68	137
1	1	0	0	1	64	1366	1048	1230	81	137
1	0	0	0	4	64	1348	1048	1208	80	136
4	0	0	0	1	64	1934	1384	2094	68	140
2	1	0	0	1	64	1864	1361	1766	69	137
2	1	1	0	1	64	1947	1395	1964	67	136
4	1	1	0	1	64	2299	1589	2470	67	134
2	1	1	0	2	64	1893	1377	2002	68	135
2	1	0	0	2	64	1796	1359	17777	67	134
4	1	1	0	4	64	2382	1603	2585	68	136
2	1	1	1	1	64	2113	1603	1968	68	136
4	1	1	1	1	64	2481	1794	2474	67	135
2	1	1	1	2	64	2139	1585	2006	69	134
2	1	0	1	2	64	2065	1587	1781	68	135
4	1	1	1	4	64	2538	1811	2590	68	134

Table 14: Performance and Resource Utilization Benchmarks (Virtex-II Pro)

Parameter Values						Device Resources			Performance	
C_NUM_CHANNELS	C_INCLUDE_OPB_IPIF	C_INCLUDE_OPB_BURST_SUPPORT	C_REG_DIMM	C_NUM_BANKS_MEM	C_DDR_DWIDTH	Slices	Slice FFs	4-input LUTs	MCH/OPB Clock Fmax (MHz)	DDR2 Device Clock Fmax (MHz)
1	1	0	0	1	16	767	579	822	101	203
1	0	0	0	4	16	783	588	876	102	202
4	0	0	0	1	16	1400	918	1750	100	203
2	1	0	0	1	16	1290	876	1362	101	204
2	1	1	0	1	16	1350	908	1573	100	204
4	1	1	0	1	16	1707	1129	2109	100	202
2	1	1	0	2	16	1328	899	1617	100	204
2	1	0	0	2	16	1309	880	1419	100	203
4	1	1	0	4	16	1678	1137	2236	100	200
2	1	1	1	1	16	1426	966	1577	100	202
4	1	1	1	1	16	1742	1186	2113	100	202
2	1	1	1	2	16	1378	956	1622	100	202
2	1	0	1	2	16	1260	937	1423	100	201
4	1	1	1	4	16	1749	1194	2240	100	200
1	1	0	0	1	32	1007	722	952	100	204
1	0	0	0	4	32	945	727	946	100	204
4	0	0	0	1	32	1575	1048	1809	100	203
2	1	0	0	1	32	1223	1006	1443	100	205
2	1	1	0	1	32	1483	1042	1648	100	204
4	1	1	0	1	32	1768	1261	2186	100	202
2	1	1	0	2	32	1411	1033	1680	100	202
2	1	0	0	2	32	1393	1010	1488	100	202
4	1	1	0	4	32	1886	1274	2318	100	200
2	1	1	1	1	32	1548	1164	1652	100	200
4	1	1	1	1	32	1782	1383	2190	100	200
2	1	1	1	2	32	1587	1160	1689	100	200

Table 14: Performance and Resource Utilization Benchmarks (Virtex-II Pro)

Parameter Values						Device Resources			Performance	
C_NUM_CHANNELS	C_INCLUDE_OPB_IPIF	C_INCLUDE_OPB_BURST_SUPPORT	C_REG_DIMM	C_NUM_BANKS_MEM	C_DDR_DWIDTH	Slices	Slice FFs	4-input LUTs	MCH/OPB Clock Fmax (MHz)	DDR2 Device Clock Fmax (MHz)
2	1	0	1	2	32	1449	1130	1492	100	204
4	1	1	1	4	32	1959	1382	2314	100	200
1	1	0	0	1	64	1305	1044	1190	100	200
1	0	0	0	4	64	1305	1056	1193	100	200
4	0	0	0	1	64	1815	1365	2061	100	201
2	1	0	0	1	64	1662	1328	1686	100	202
2	1	1	0	1	64	1750	1369	1920	100	202
4	1	1	0	1	64	2114	1589	2445	100	200
2	1	1	0	2	64	1787	1589	1978	100	200
2	1	0	0	2	64	1730	1341	1770	101	200
4	1	1	0	4	64	2198	1591	2547	100	202
2	1	1	1	1	64	1949	1577	1924	100	202
4	1	1	1	1	64	2281	1797	2449	100	203
2	1	1	1	2	64	1867	1571	1982	100	204
2	1	0	1	2	64	1876	1549	1774	100	202
4	1	1	1	4	64	2375	1821	2603	100	200

Table 15: Performance and Resource Utilization Benchmarks (Virtex-4)

Parameter Values						Device Resources			Performance	
C_NUM_CHANNELS	C_INCLUDE_OPB_IPIF	C_INCLUDE_OPB_BURST_SUPPORT	C_REG_DIMM	C_NUM_BANKS_MEM	C_DDR_DWIDTH	Slices	Slice FFs	4-input LUTs	MCH/OPB Clock Fmax (MHz)	DDR2 Device Clock Fmax (MHz)
1	1	0	0	1	16	1054	893	1190	127	226
1	0	0	0	4	16	1134	901	1204	116	216
4	0	0	0	1	16	1714	1237	2059	101	209
2	1	0	0	1	16	1594	1193	1702	107	229
2	1	1	0	1	16	1624	1217	1925	105	206
4	1	1	0	1	16	2104	1433	2454	101	207
2	1	1	0	2	16	1756	1213	1978	105	214
2	1	0	0	2	16	1670	1207	1766	102	213
4	1	1	0	4	16	2143	1450	2588	101	205
2	1	1	1	1	16	1744	1275	1931	106	203
4	1	1	1	1	16	2024	1491	2460	103	206
2	1	1	1	2	16	1847	1271	1984	104	203
2	1	0	1	2	16	1671	1265	1732	103	204
4	1	1	1	4	16	2114	1508	2594	102	203
1	1	0	0	1	32	1599	1270	1552	114	203
1	0	0	0	4	32	1513	1276	1579	126	202
4	0	0	0	1	32	2122	1607	2448	107	203
2	1	0	0	1	32	2016	1570	2068	103	204
2	1	1	0	1	32	2110	1600	2285	101	205
4	1	1	0	1	32	2532	1820	2833	102	211
2	1	1	0	2	32	2019	1590	2331	102	200
2	1	0	0	2	32	1911	1586	2118	105	206
4	1	1	0	4	32	2354	1621	2964	101	209
2	1	1	1	1	32	2032	1703	2295	106	212
4	1	1	1	1	32	2641	1923	2843	101	205
2	1	1	1	2	32	2262	1695	2341	102	202

Table 15: Performance and Resource Utilization Benchmarks (Virtex-4) (Continued)

Parameter Values						Device Resources			Performance	
C_NUM_CHANNELS	C_INCLUDE_OPB_IPIF	C_INCLUDE_OPB_BURST_SUPPORT	C_REG_DIMM	C_NUM_BANKS_MEM	C_DDR_DWIDTH	Slices	Slice FFs	4-input LUTs	MCH/OPB Clock Fmax (MHz)	DDR2 Device Clock Fmax (MHz)
2	1	0	1	2	32	2205	1691	2128	106	201
4	1	1	1	4	32	2506	1935	2974	101	223
1	1	0	0	1	64	2302	2165	2442	108	205
1	0	0	0	4	64	2256	2171	2467	121	202
4	0	0	0	1	64	2941	2511	3328	102	203
2	1	0	0	1	64	2742	2467	2954	104	201
2	1	1	0	1	64	3171	2500	3179	102	208
4	1	1	0	1	64	3301	2717	3739	101	209
2	1	1	0	2	64	2850	2485	3225	102	202
2	1	0	0	2	64	2790	2485	3014	102	205
4	1	1	0	4	64	3223	2727	3844	102	206
2	1	1	1	1	64	3054	2723	3197	105	206
4	1	1	1	1	64	3558	2940	3757	102	203
2	1	1	1	2	64	3110	2708	3243	103	203
2	1	0	1	2	64	2911	2708	3032	105	208
4	1	1	1	4	64	3446	2949	3843	103	201

Specification Exceptions

1. Additive latency feature of DDR2 SDRAM memory is not supported. Additive latency of DDR2 memories is set to zero which causes read latencies of DDR2 SDRAM memory is same as its CAS latency.
2. Off Chip Driver (OCD) calibration of DDR2 SDRAM memory is not supported.

Reference Documents

The following documents contain reference information important to understanding the MCH OPB DDR2 SDRAM Controller design:

1. MicroBlaze Processor Reference Guide UG081
2. MCH OPB IPIF Specification DS494
3. JEDEC's DDR2 SDRAM specification JESD79-2A
4. OPB IPIF Specification DS414

5. PLB DDR2 SDRAM Specification DS326
6. MCH OPB DDR Specification DS496

Revision History

Date	Version	Revision	Ed
12/21/05	1.0	Initial release	PK
03/17/06	1.1	Updated document with resource utilization and performance table.	PK
03/20/06	1.2	Updated the document with timing diagrams	bsb

Discontinued IP